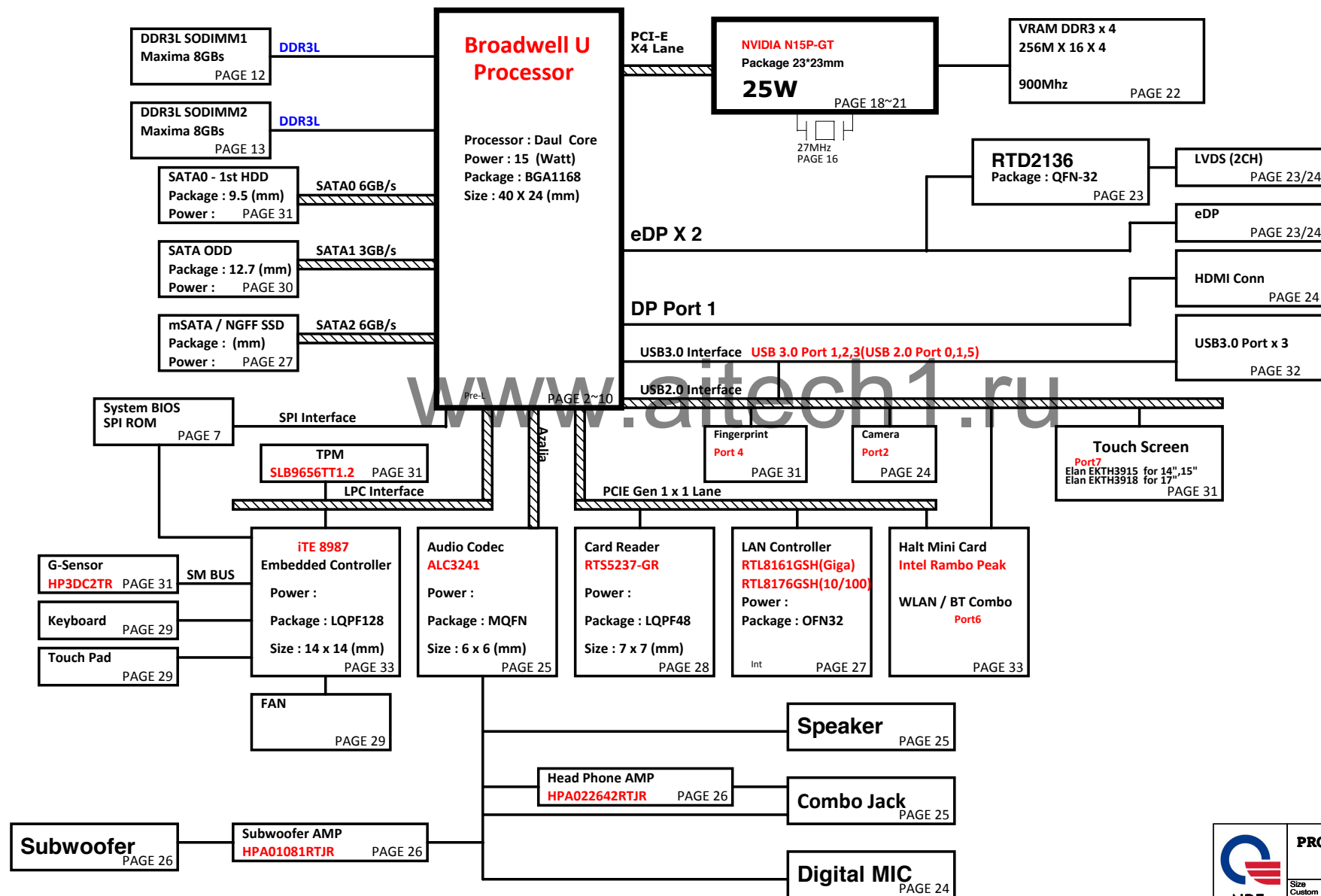


# DIS (14" / 15" / 17") Lay-Vine Intel Crescent Bay ULT Platform Block Diagram

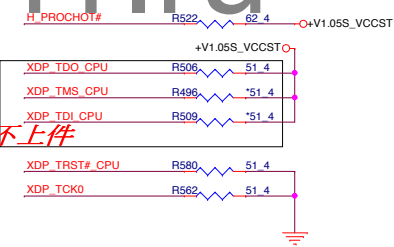
PCB 6L STACK UP

LAYER 1 : TOP  
LAYER 2 : SGND  
LAYER 3 : IN1(High)  
LAYER 4 : IN2(Low)  
LAYER 5 : SVCC  
LAYER 6 : BOT

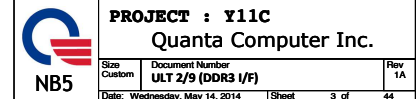


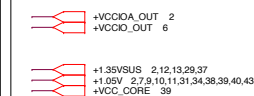


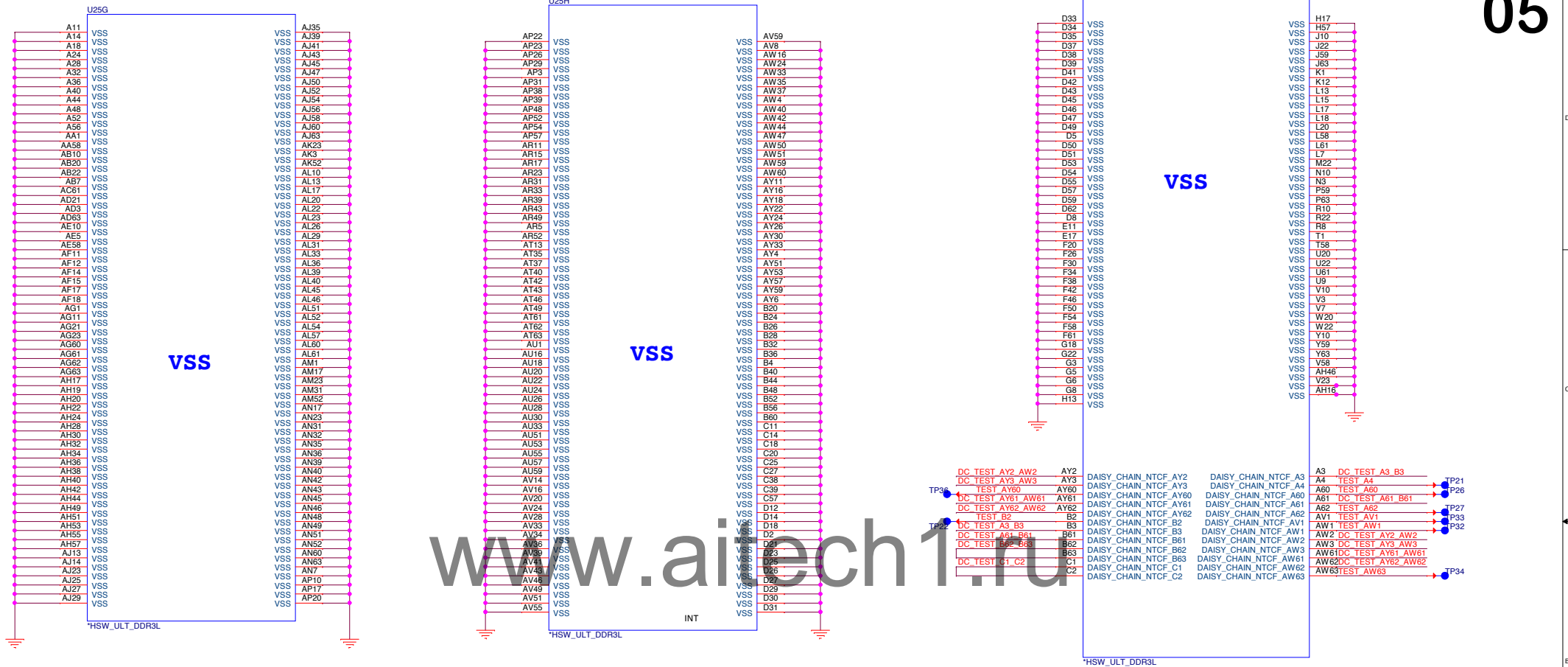
### Processor pull-up (CPU)



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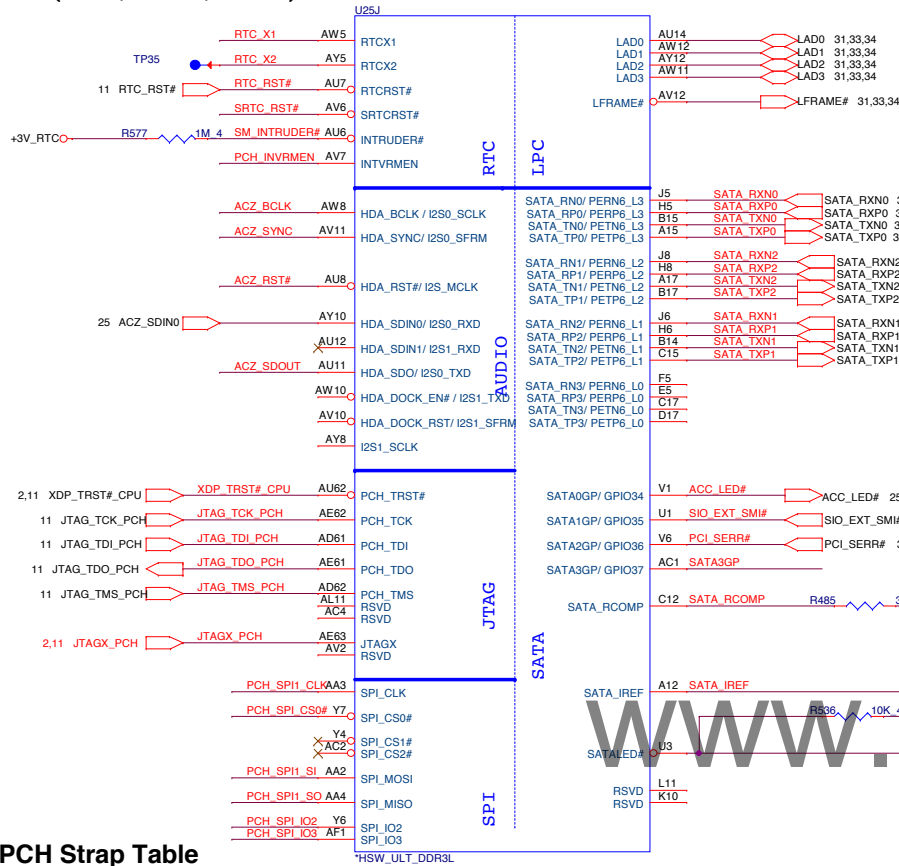




















# Lynx Point-LP Platform Controller Hub (HDA, JTAG, SATA)



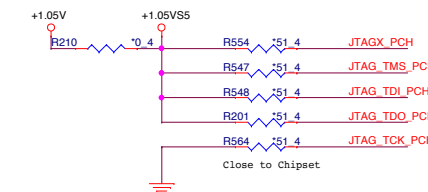
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit				
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode					
SDIO_D0 /GPIO66	Top-Block Swap	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)					
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC0  330K 4  PCH_INVRMEN				
HDA_SDO /I2S0_TXD	Flash Descriptor Security Only for Interposer	PWROK	0 = Default (weak pull-down 20K) 1 = Can be Overriden	34 GPIO3_EC  R581  1K 4  ACZ_SDOOUT				
GSPI0_MOSI /GPIO86	Boot BIOS Selection	PWROK	<table border="1"><thead><tr><th>GNT0#</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>LPC SPI(Default)</td></tr></tbody></table>	GNT0#	Boot Location	1	LPC SPI(Default)	
GNT0#	Boot Location							
1	LPC SPI(Default)							
GPIO15	TLS Confidentiality	PWROK	0 = ME Crypto Transport Layer Security cipher suite with no confidentiality(Default) 1 = Intel ME Crypto TLS cipher suite with confidentiality					
DSWVRMEN	Deep Sx Well On-Die Voltage Regulator Enable	ALWAYS	Should be always pull-up	+3V_RTC0  R576  330K 4  DSWVRMEN 6				
				<div>34 PCH_SPI_CS0#_R  PCH_SPI_CS0#_R</div> <div>34 PCH_SPI1_CLK_R  PCH_SPI1_CLK_R</div> <div>34 PCH_SPI1_SI_R  PCH_SPI1_SI_R</div> <div>34 PCH_SPI1_SO_R  PCH_SPI1_SO_R</div>				

HDD (SATA3 6.0Gb/s)

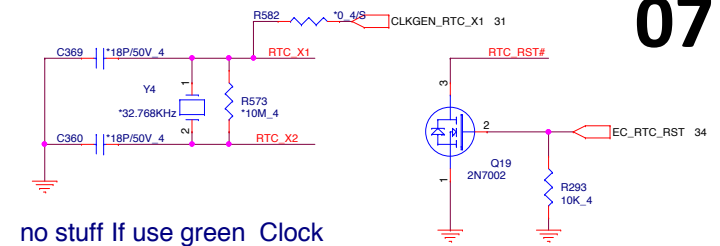
ODD (SATA2 3.0Gb/s)

mSATA / NGFF (SATA4 6Gb/s)



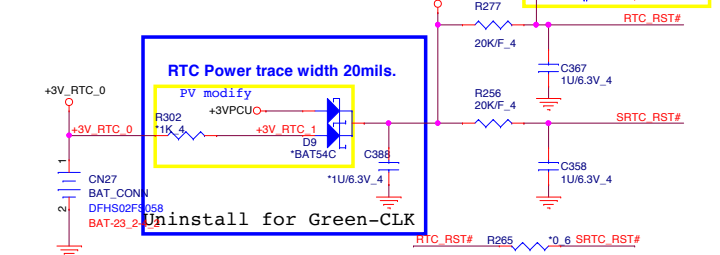
DG recommended that SATA AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

## RTC Clock 32.768KHz

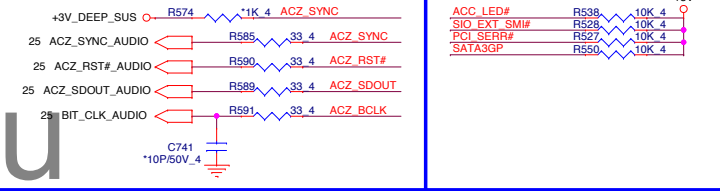


no stuff if use green Clock

## RTC Circuitry(RTC)



## HDA Bus(CLG)

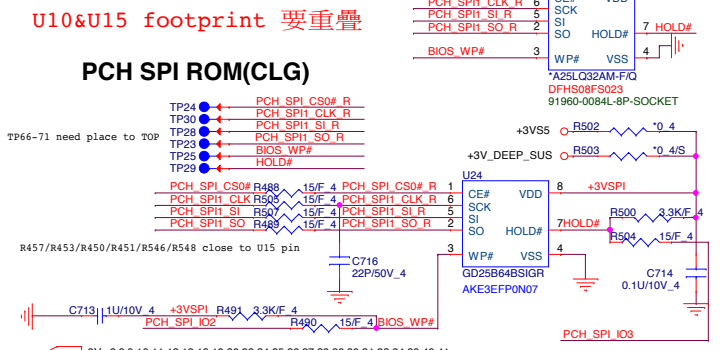


## GPIO Pull UP

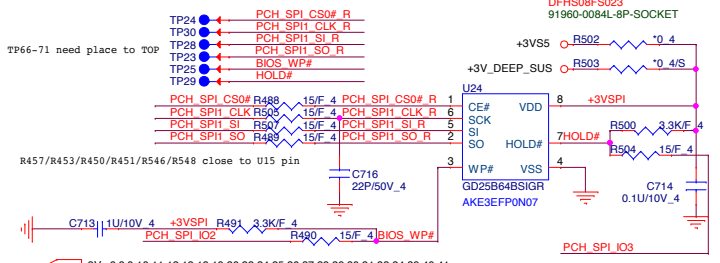


Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

## 4M SPI ROM Socket



## PCH SPI ROM(CLG)

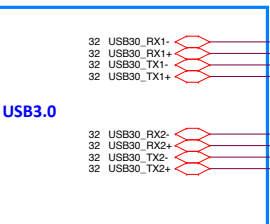
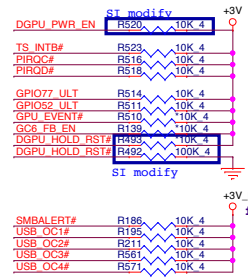


**PROJECT : Y11C**  
**Quanta Computer Inc.**  
Size Custom Document Number **ULT 6/9(SATA/HDA)** Rev 1A  
Date: Tuesday, May 27, 2014 Sheet 7 of 44

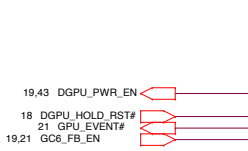


Lynx Point-LP Platform Controller Hub  
(HDA, JTAG, SATA)

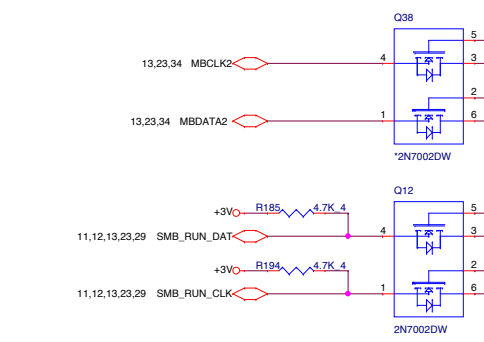
PCI/USBOC# Pull-up(CLG)



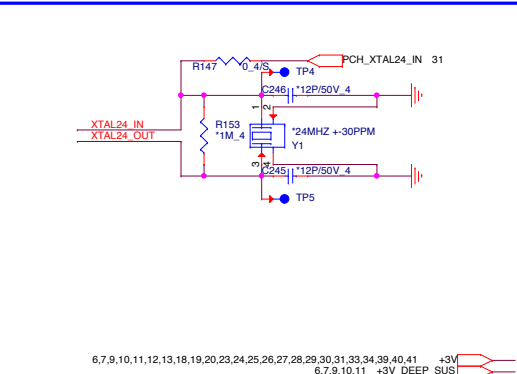
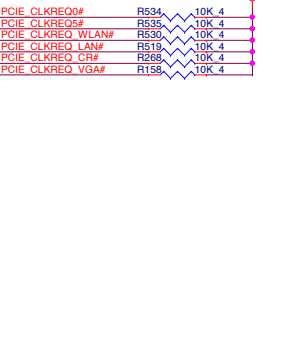
20111130 Modify USB3.0 for HM70



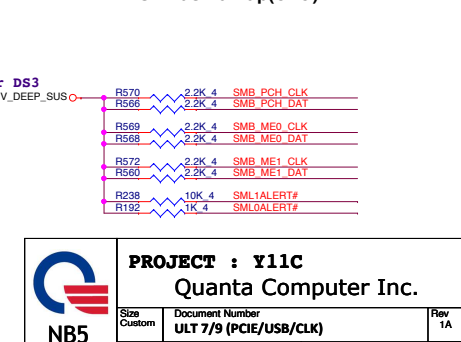
SMBus/Pull-up(CLG)



CLK\_REQ/Strap Pin(CLG)



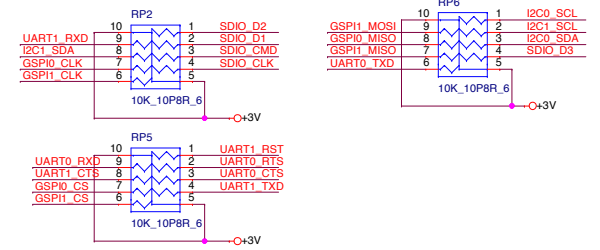
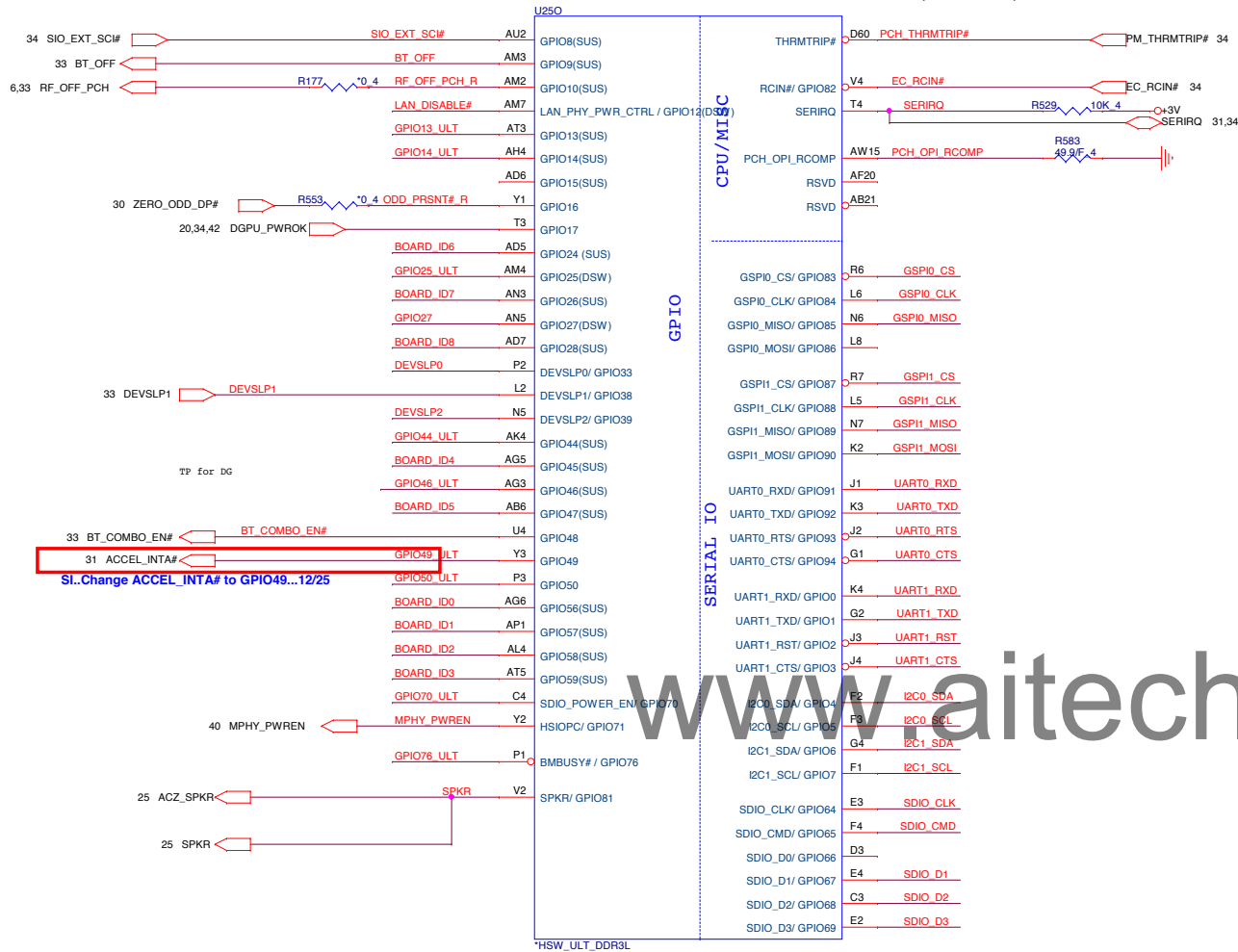
SMBus/Pull-up(CLG)





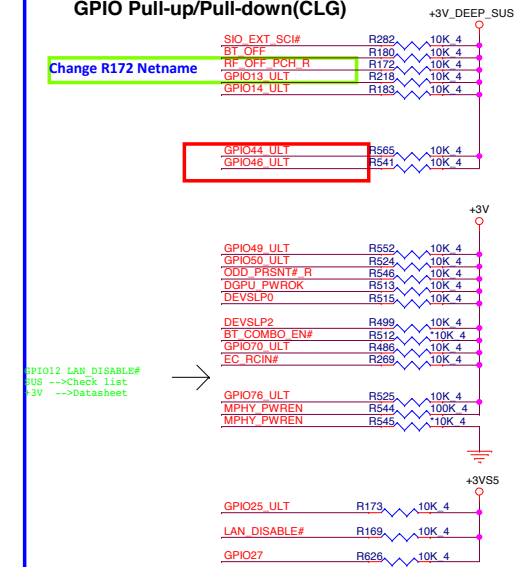
# Lynx Point-LP Platform Controller Hub (HDA,JTAG,SATA) Haswell (GPIO)

09

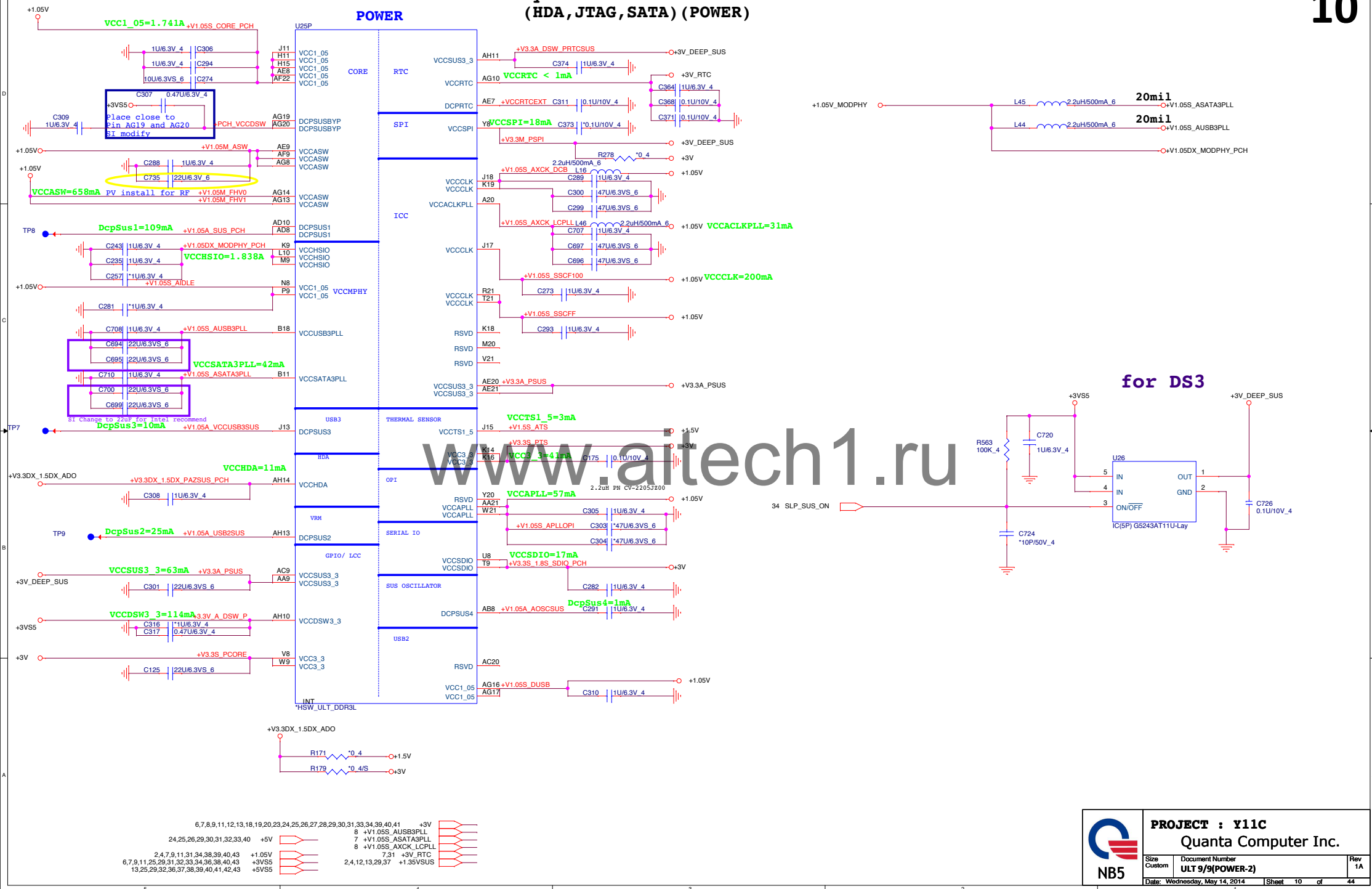


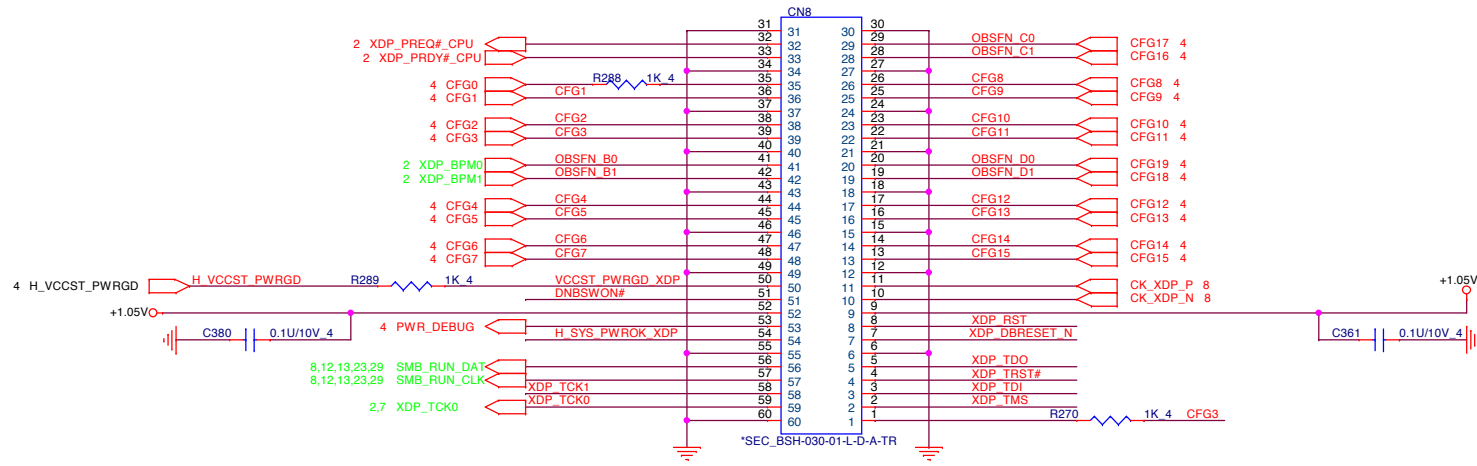
## GPIO Pull-up/Pull-down(CLG)

Change R172 Netname

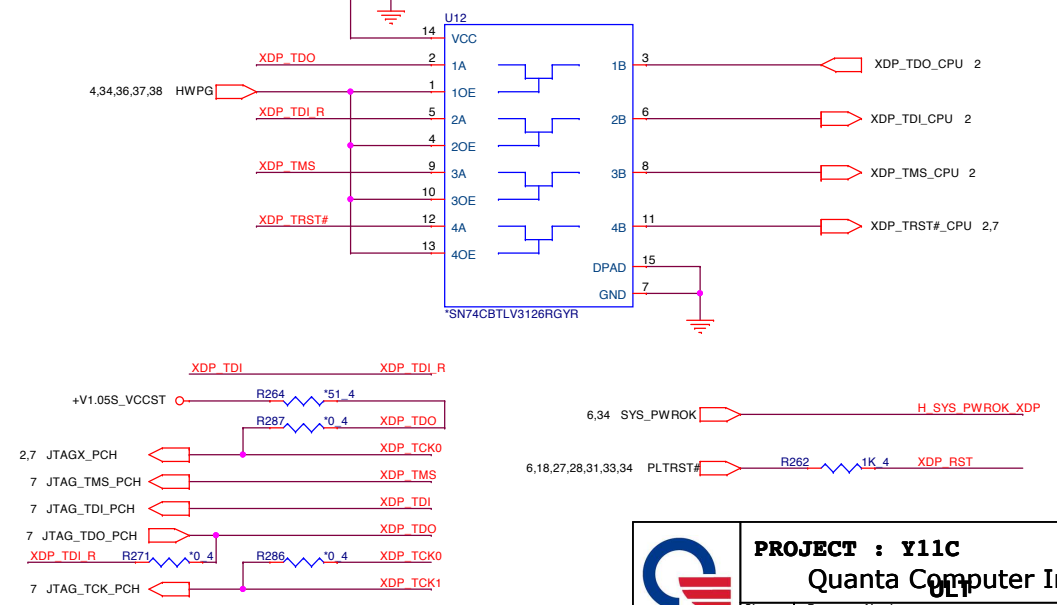
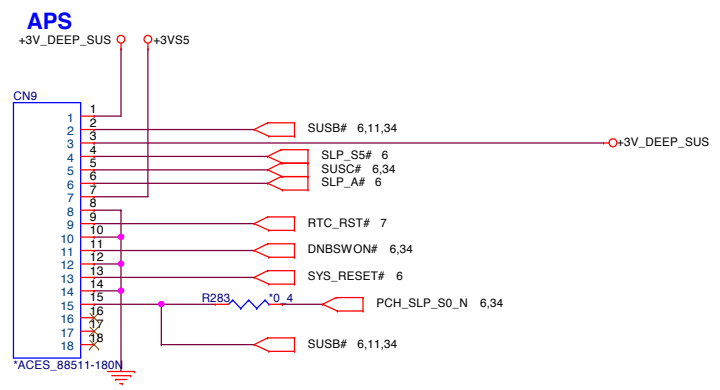


# Lynx Point-LP Platform Controller Hub (HDA, JTAG, SATA) (POWER)

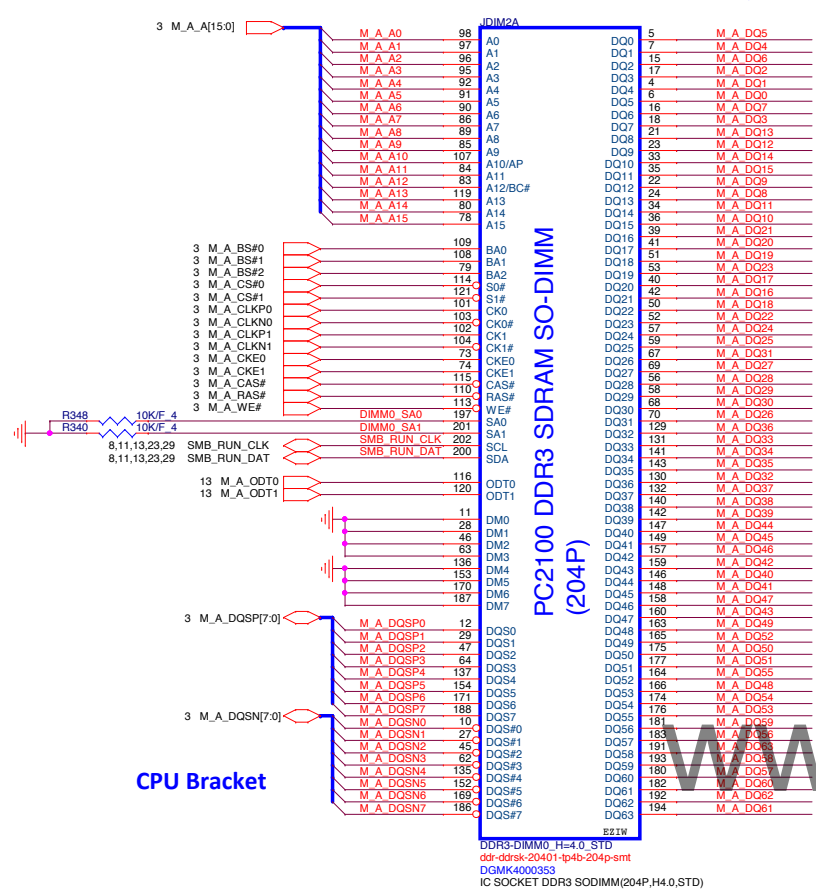




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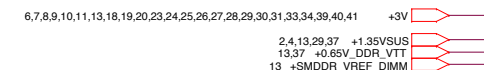
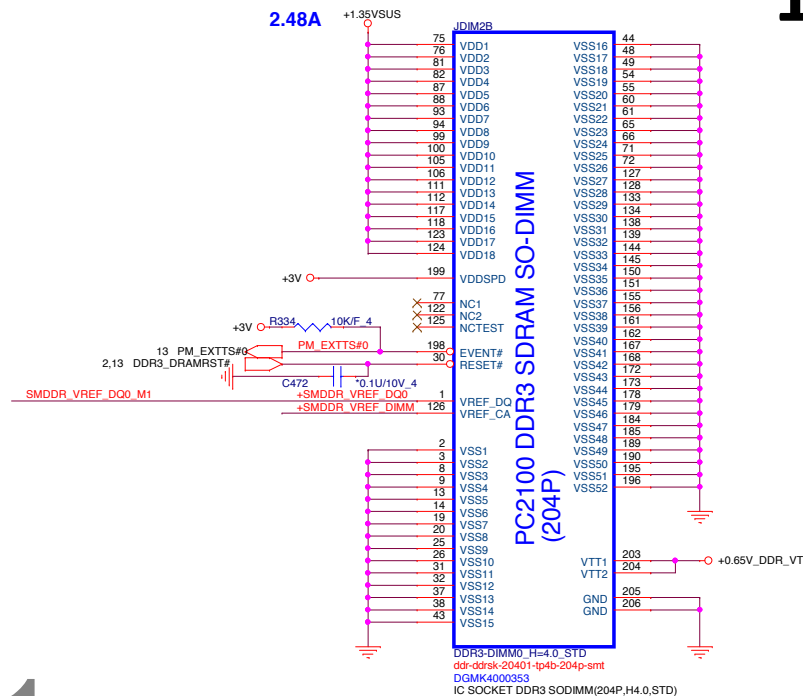


## DIMM &amp; Footprint 同Joshua提供

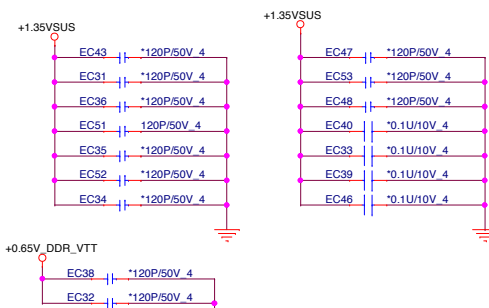


CPU Bracket

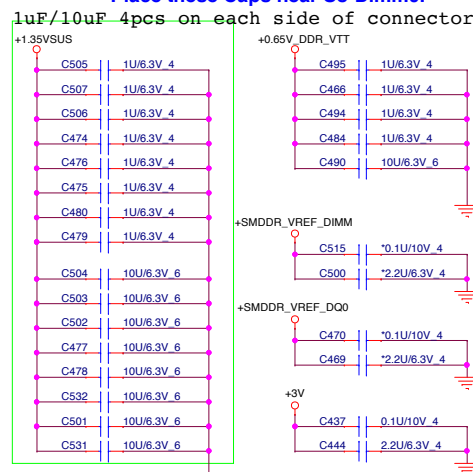
M\_A\_DQ[63:0] 3



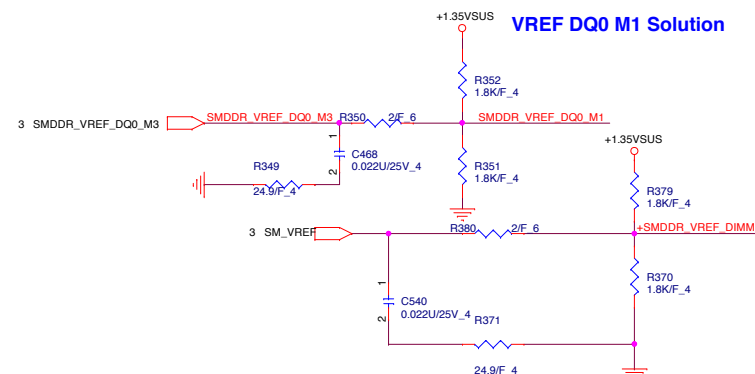
## For EMI RESERVE



## Place these Caps near So-Dimm0.

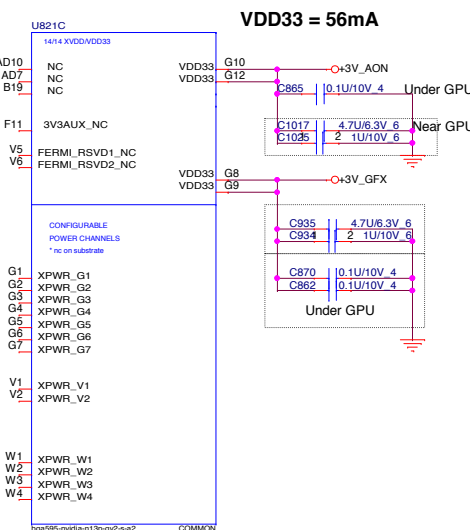
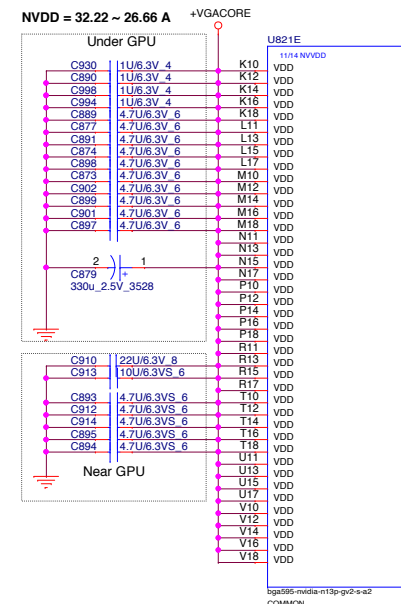
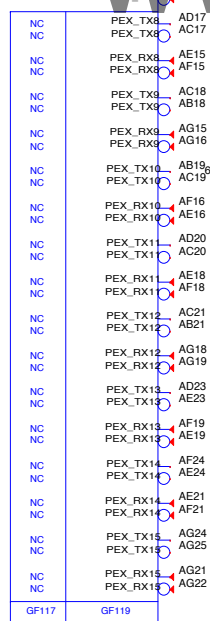
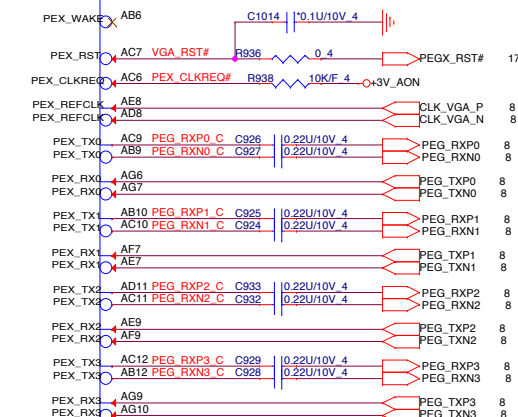
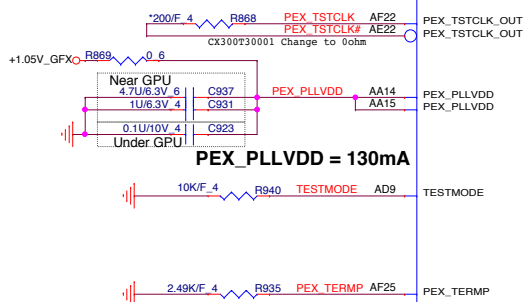
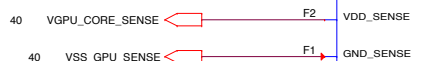


## VREF DQ0 M1 Solution





The diagram illustrates a 16-core GPU architecture. It is divided into two main sections: 'Near GPU' and 'Under GPU'. The 'Near GPU' section contains 8 cores (C1018 to C1024) and 8 ALUs (AA10 to AA19). The 'Under GPU' section contains 8 cores (C905 to C917) and 8 ALUs (AB22 to AB27). A central bus connects the two sections. A red arrow labeled '+1.05V\_GFX' points to the top of the 'Near GPU' section.



ALL 3.3V  
+3VGFX & +3V3\_AON

NVVDD  
+VGACORE

PEX\_VDD  
+1.05V\_GFX

FBVDDQ  
+1.35V GFX

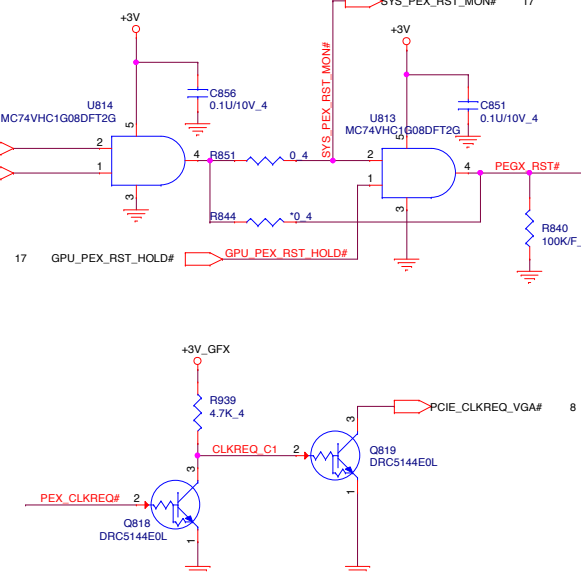
$t > 0$

$t \geq 0$

First Rail to Power Down

Last Rail to Power Down

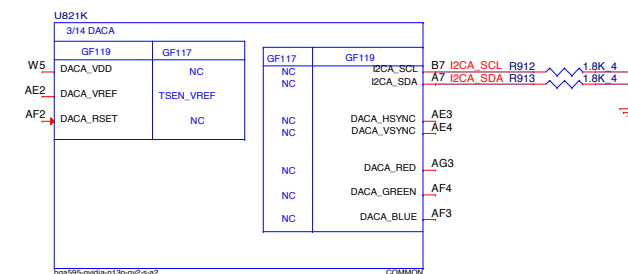
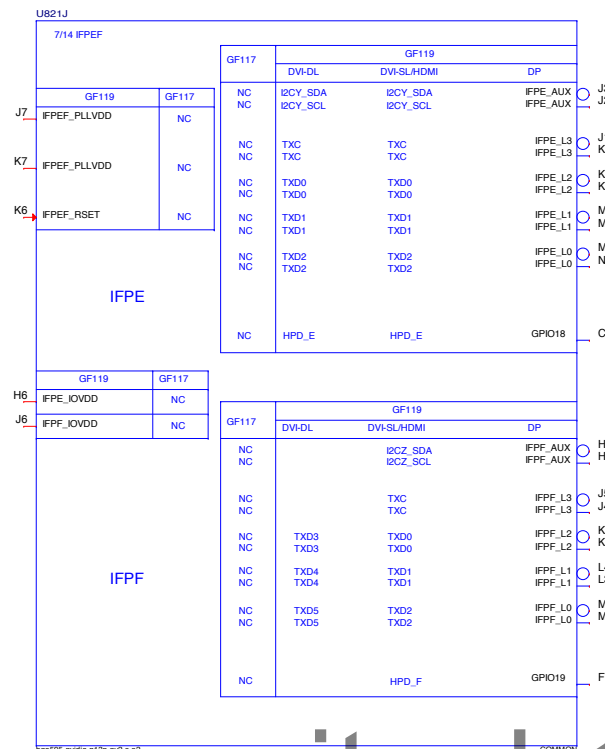
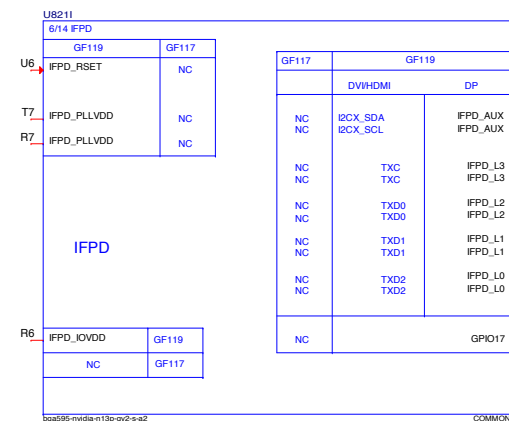
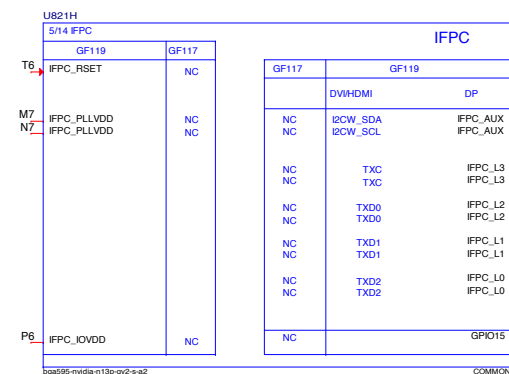
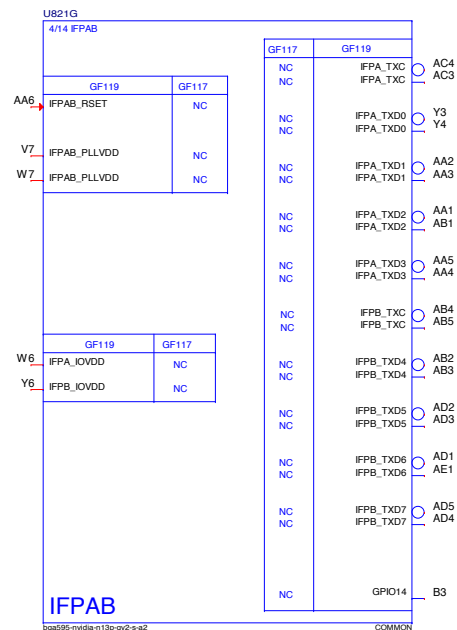
$t_{\text{Power-OFF}} < 10 \text{ ms}$











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PLLVD = 38mA

+1.05V\_GFX

L100P5 PBV16080BT-300T-N

C872 0.1U/10V 4

C875 22U/6.3V 6

SP\_PLLVDD = 17mA

+1.05V\_GFX

L100P5 PBV16080BT-300T-N

C872 0.1U/10V 4

C875 22U/6.3V 6

VID\_PLLVDD = 41mA

+1.05V\_GFX

L100P5 PBV16080BT-300T-N

C872 0.1U/10V 4

C875 22U/6.3V 6

DB-->SI change 10/25

Use G-CLK

CLK\_27M\_XTAL\_IN

R898 0.4

27M\_XTAL\_IN\_R

XTALSSIN

XTALOUTBUFF

C10 BXTALOUT

R906 10K/F 4

XTALOUT

B10 27M\_XTAL\_OUT

COMMON

bga595-mvda-n13p-gv2-s-a2

U821M

9/14 XTAL\_PLL

PLLVD

SP\_PLLVDD

VID\_PLLVDD

NC

GF119

GF117

COMMON

bga595-mvda-n13p-gv2-s-a2

U821M

9/14 XTAL\_PLL

PLLVD

SP\_PLLVDD

VID\_PLLVDD

NC

GF119

GF117

COMMON

bga595-mvda-n13p-gv2-s-a2

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VID\_PLLVDD

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PLLVD

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PLLVD

SP\_PLLVDD

VID\_PLLVDD

NC

GF119

GF117

COMMON

bga595-mvda-n13p-gv2-s-a2

U821M

9/14 XTAL\_PLL

PLLVD

SP\_PLLVDD

VID\_PLLVDD

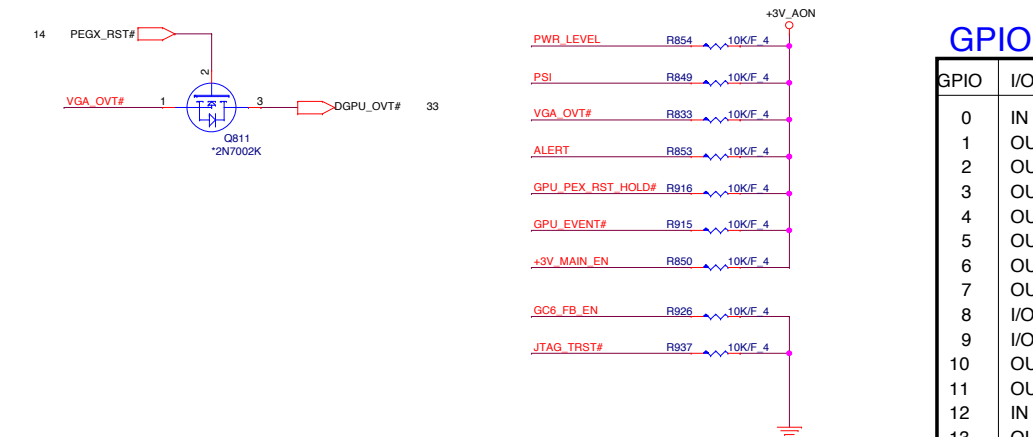
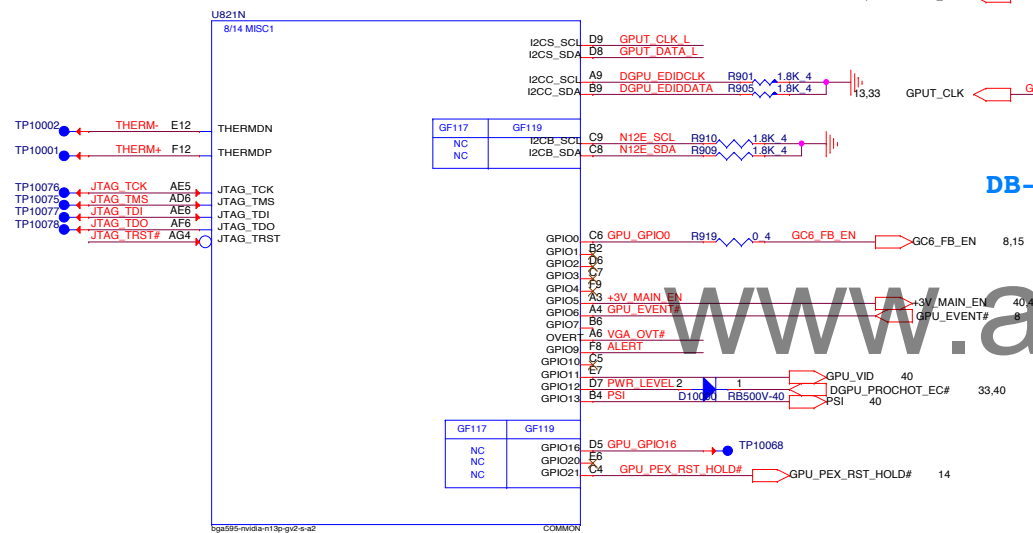
NC

GF119

GF117

COMMON

bga595-mvda-n13p-gv2-s-a2



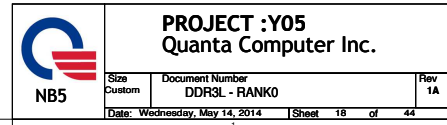
Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

```
Hynix should be 0x3, R440      20K 1%
Micro Should be 0x4, R440      24.9K 1%
Samsung Should be 0x5, R440    30.1K 1%
```

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	QCI P/N	QBC	TOP B/S
0000	DDR3L 256Mx16, 64bit, 4Gb,900MHz	Micron	MT41J256M16HA-093G:E		AKD5PZSTL01	AKD5PZSTL00
0100	DDR3L 256Mx16, 64bit, 4Gb,900MHz	HYNIX	H57C4G63AFR-11C		AKD5PGWTW08	AKD5PGWTW07
0101	DDR3L 256Mx16, 64bit, 4Gb,900MHz	SAMSUNG	K4W4G1646D-BC1A	AKD5PGWT500	AKD5PGWT501	AKD5PGWT502

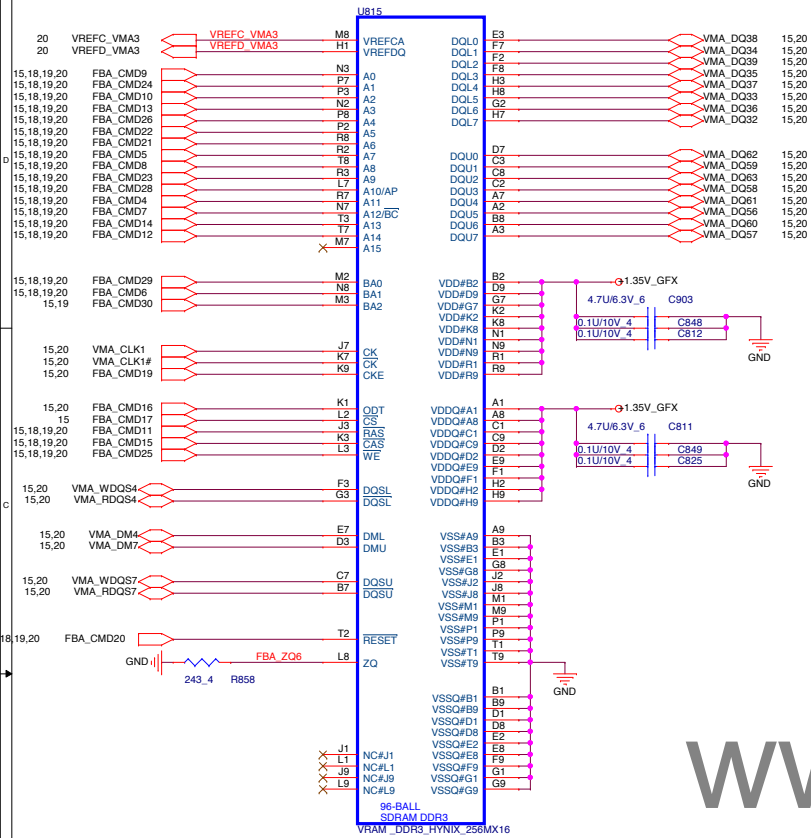
## GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D_VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMORY_VREF CONTROL
11	OUT	PWR_VID	GPU_CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

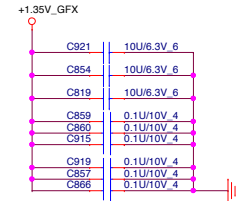
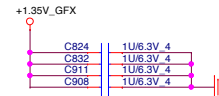
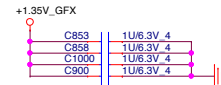
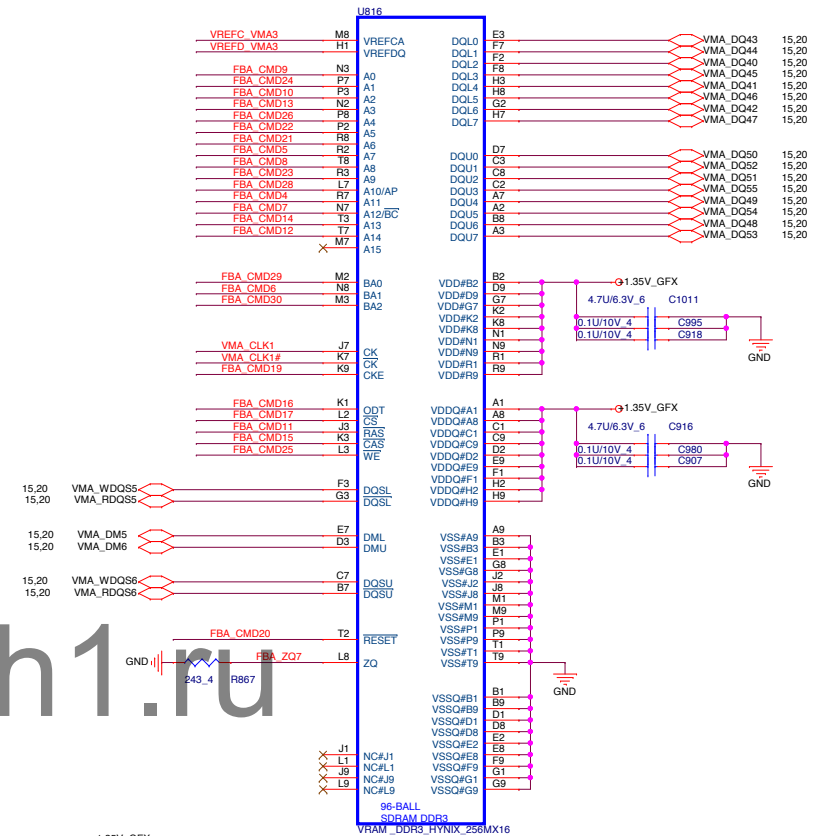









HYU 256Mx16, H5TC4G63AFR-11C QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07  
 MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00  
 SAM 256Mx16, K4W4G1646D-BC1A QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502



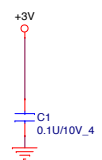
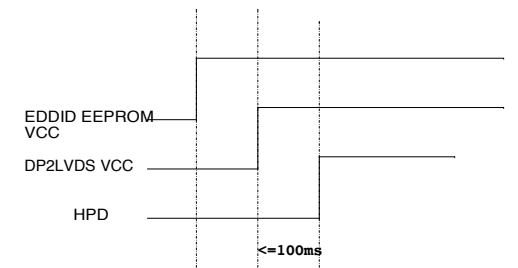
PROJECT :Y05  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3L - RANK1	1A
Date: Wednesday, May 14, 2014	Sheet 21 of 44	

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		<b>PROJECT :Y05</b> Quanta Computer Inc.	
		Size Custom	Document Number <b>N15S-GT (PCIe VF) /NVDD</b>
Date: Wednesday, May 14, 2014		Sheet 22 of 44	Rev 2A

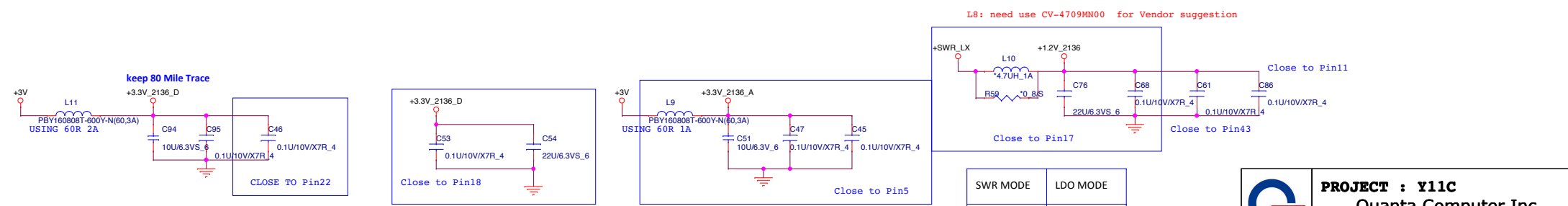





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For eDP, close to U8016

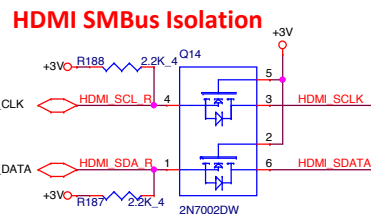
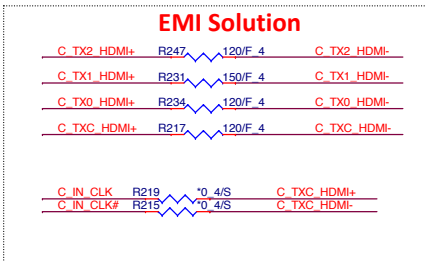
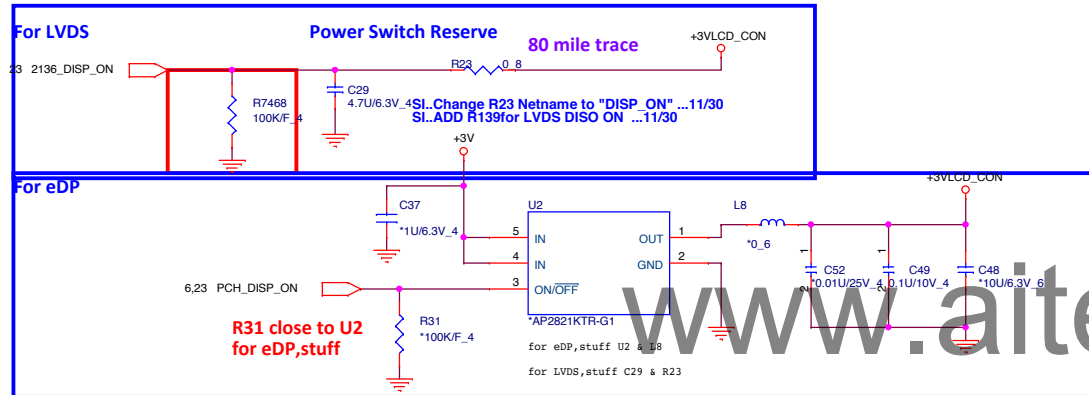
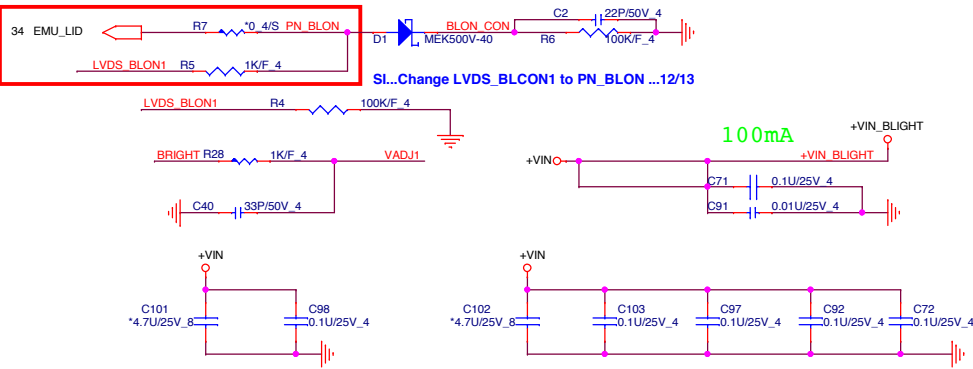
6.24	PCH_LVDS_BLON	PCH_LVDS_BLON	R50	0.4	LVDS_BLON_2136
6.24	PCH_DISP_ON	PCH_DISP_ON	R51	0.4	2136_DISP_ON
6.24	PCH_DPST_PWM	PCH_DPST_PWM	R36	0.4	2136_DPST_PWM



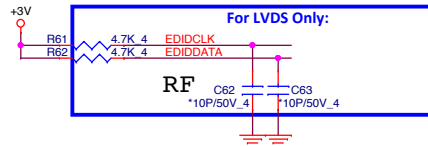
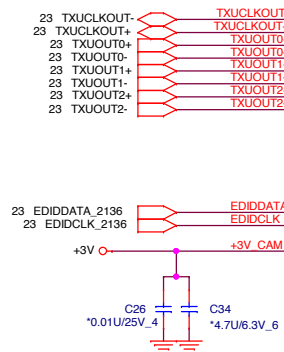
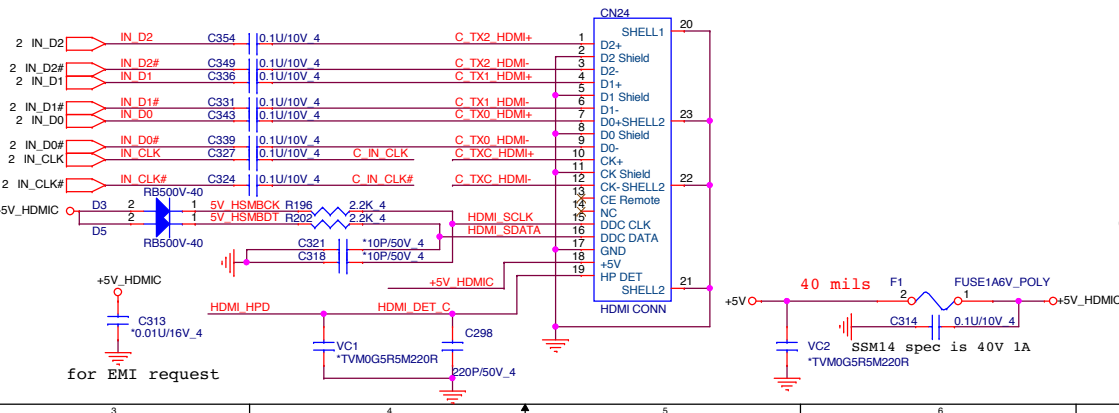
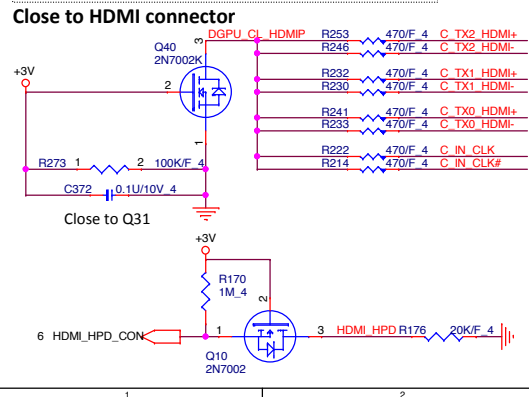
SWR MODE	LDO MODE
Stuff L8	Stuff R86

	<b>PROJECT : Y11C</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number <b>RTD2136</b>	Rev 1A
	Date: Wednesday, May 14, 2014	Sheet 23 of 44	

## LID Switch

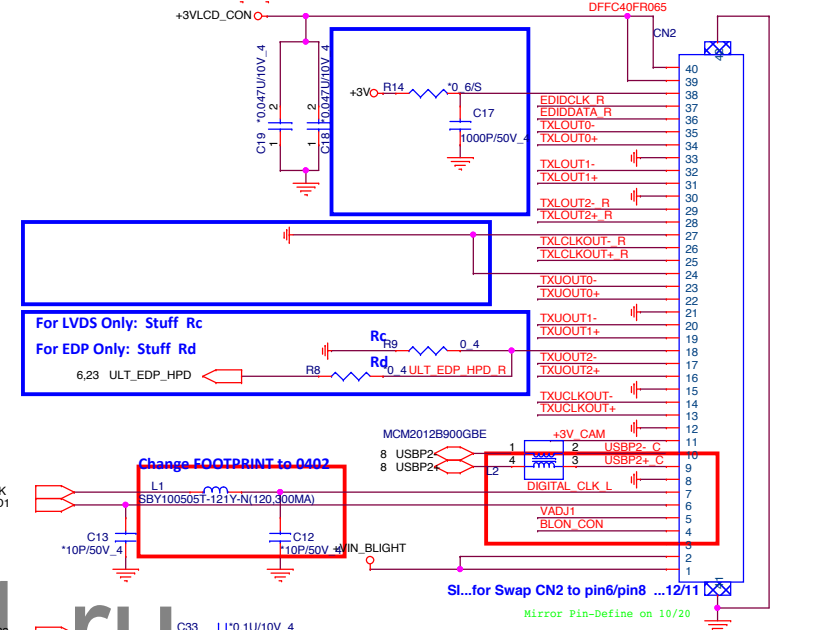


For EDP Only: stuff Cap  
For LVDS only stuff Resistor

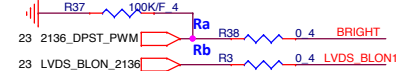


**LVDS Conn.**

24



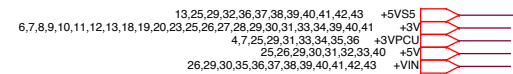
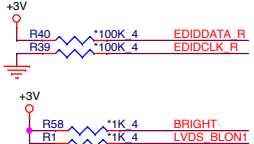
For LVDS Only: stuff Ra,Rb,Rc



For EDP Only: stuff Rd,Re,Rf



For EDP Only: stuff

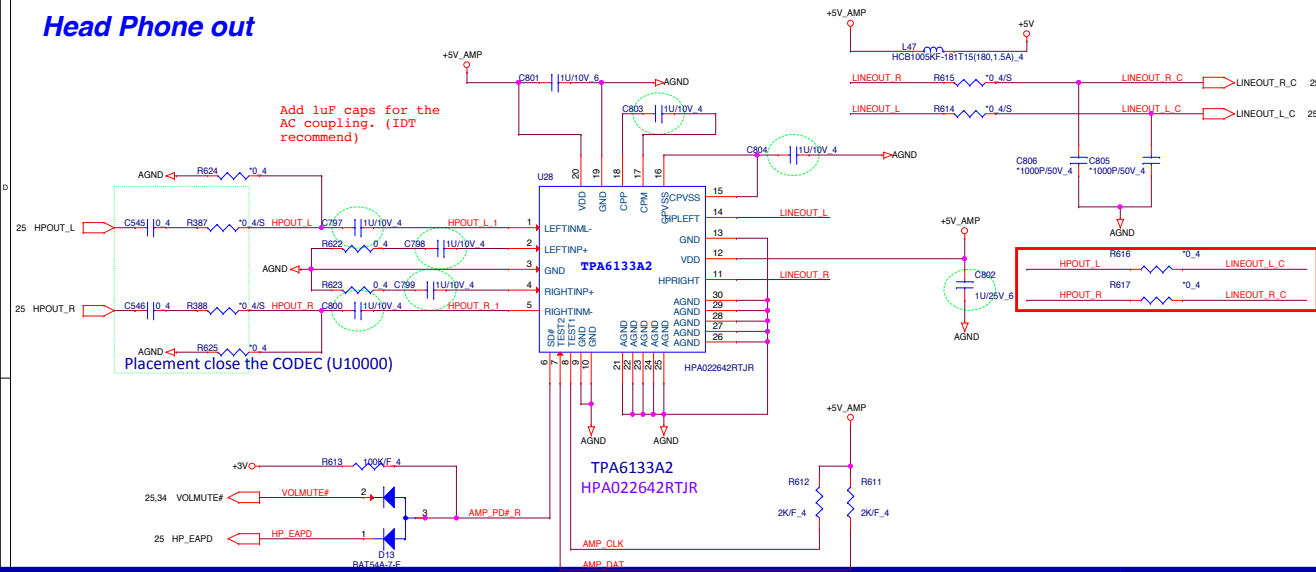


**PROJECT : Y11C**  
Quanta Computer Inc.

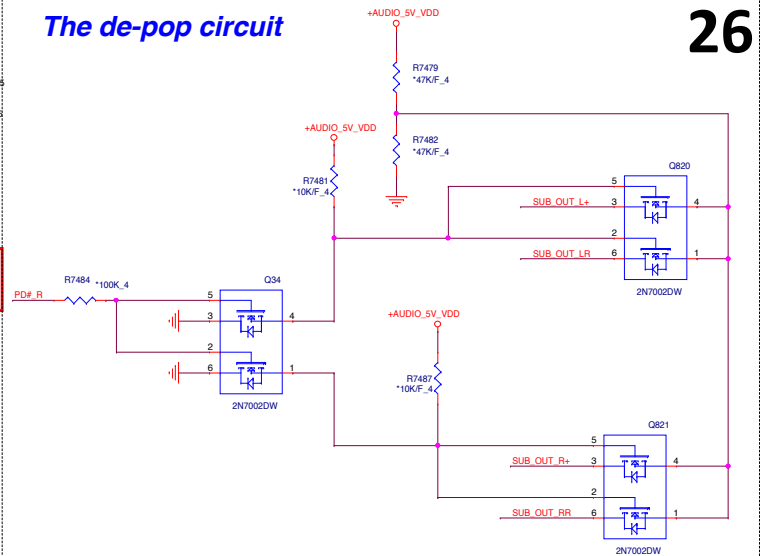
Size Custom	Document Number <b>LCD CONN/LID/CAM/D-MIC</b>
Date: Wednesday, May 14, 2014	Sheet 24 of 44



## Head Phone out

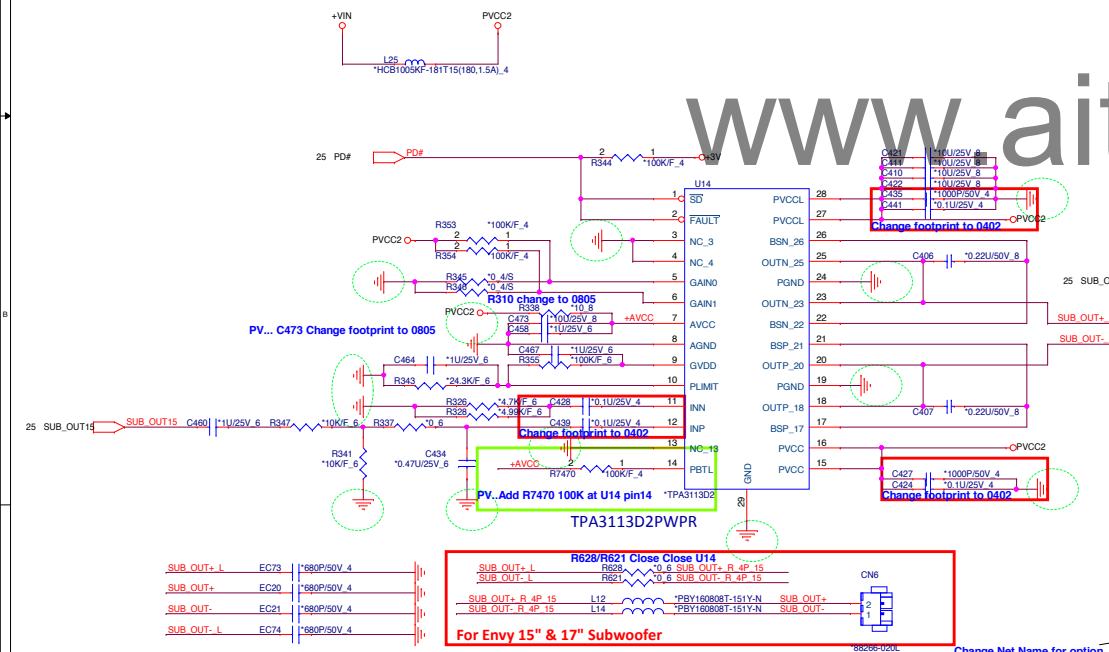


### *The de-pop circuit*

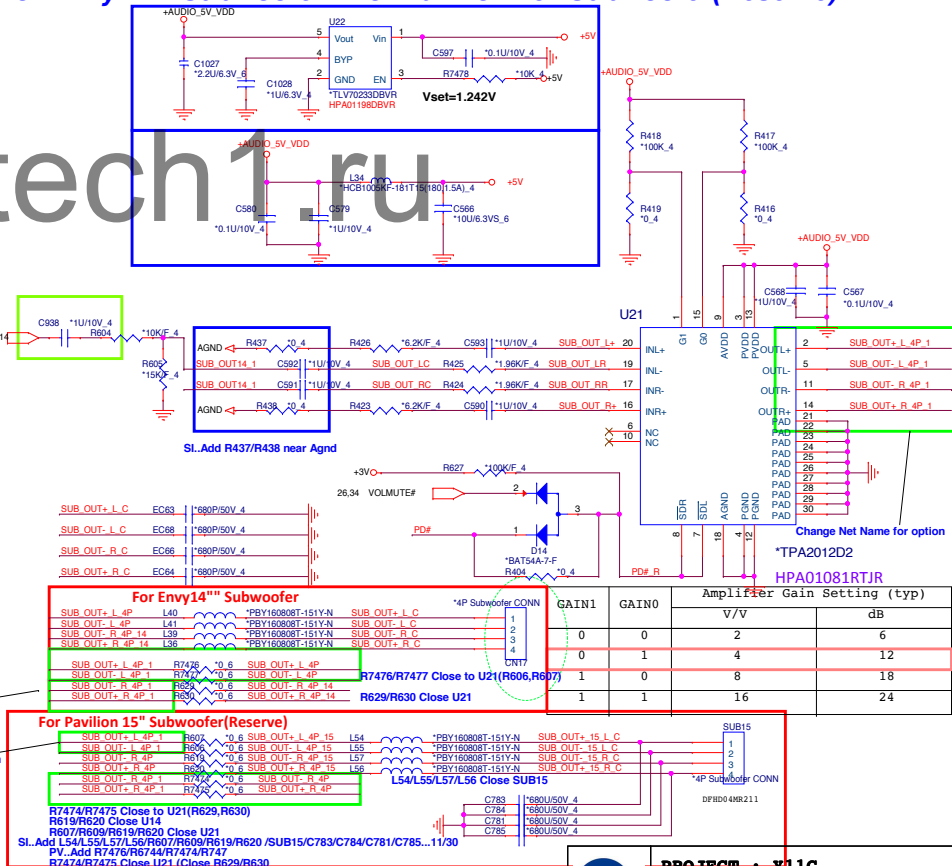


26

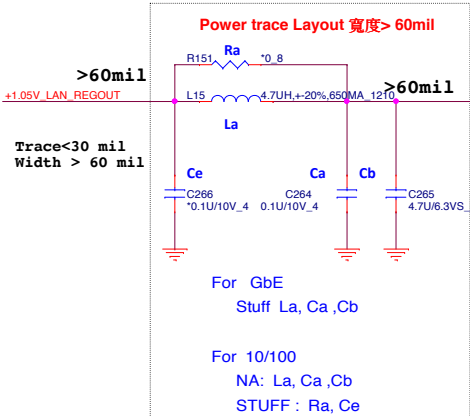
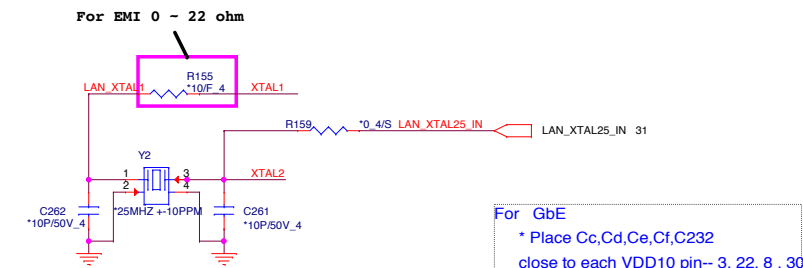
***For Envy 15" & 17" Subwoofer***



**For Envy14"" Subwoofer For Pavilion 15" Subwoofer(Reserve)**



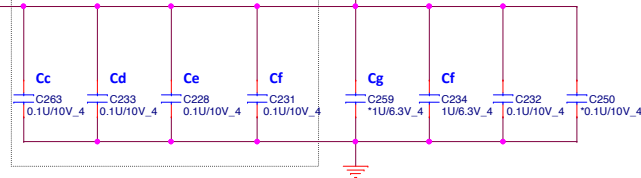
GAIN1	GAIN0	dB
0	0	20
0	1	26
1	0	32
1	1	36



For GbE

- \* Place Cc,Cd,Ce,Cf,C232 close to each VDD10 pin-- 3, 22, 8 , 30

For 10/100 NA Ce,Cf  
 \* Place Ce , Cf ,C250  
 close to each VDD10 pin-- 8, 30 only,



For GbE

- \* Place Cf close to each VDD10 pin-- 22 (reserve)

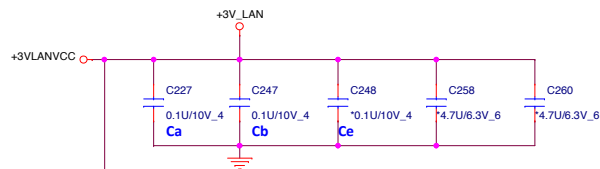
\* Place  $C_g$  close to each VDD10 pin-- 30 (reserve)

For 10/100


- \* Stuff Cb and Ce only, close to each VDD33 pin-- 23, 32

For GIGA

- \* Stuff Ca and Cb only, close to each VDD33 pin-- 11, 32



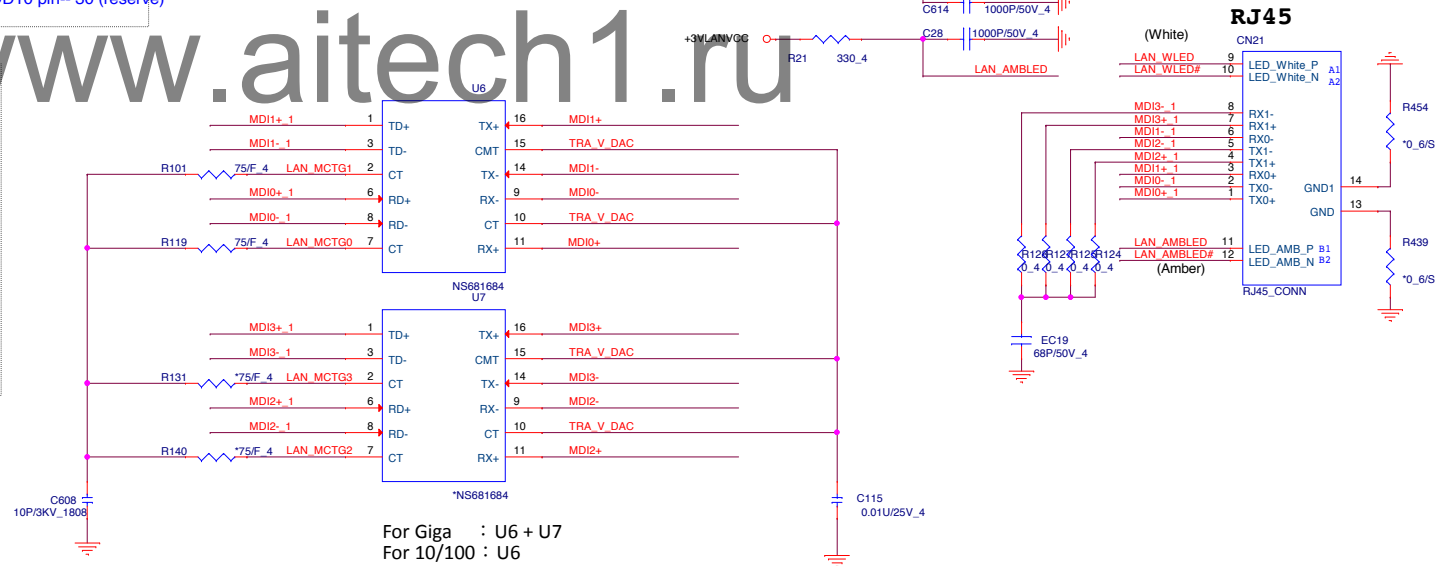
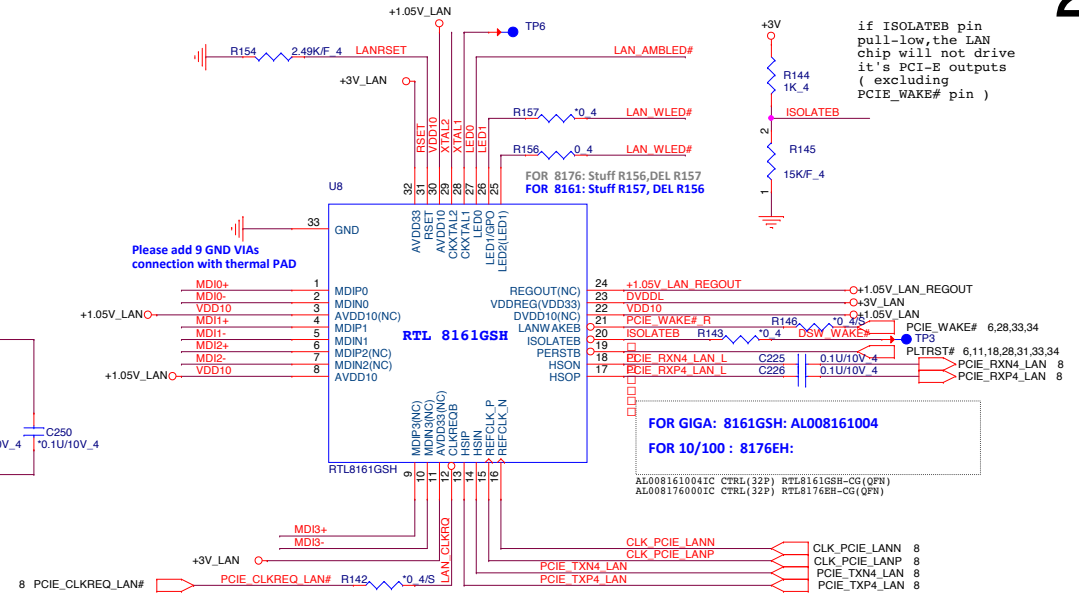
\* Place Cc and Cd close to each VDD33 pin-- 23

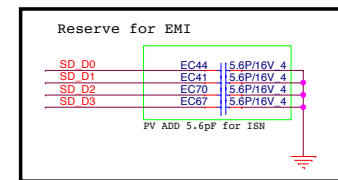
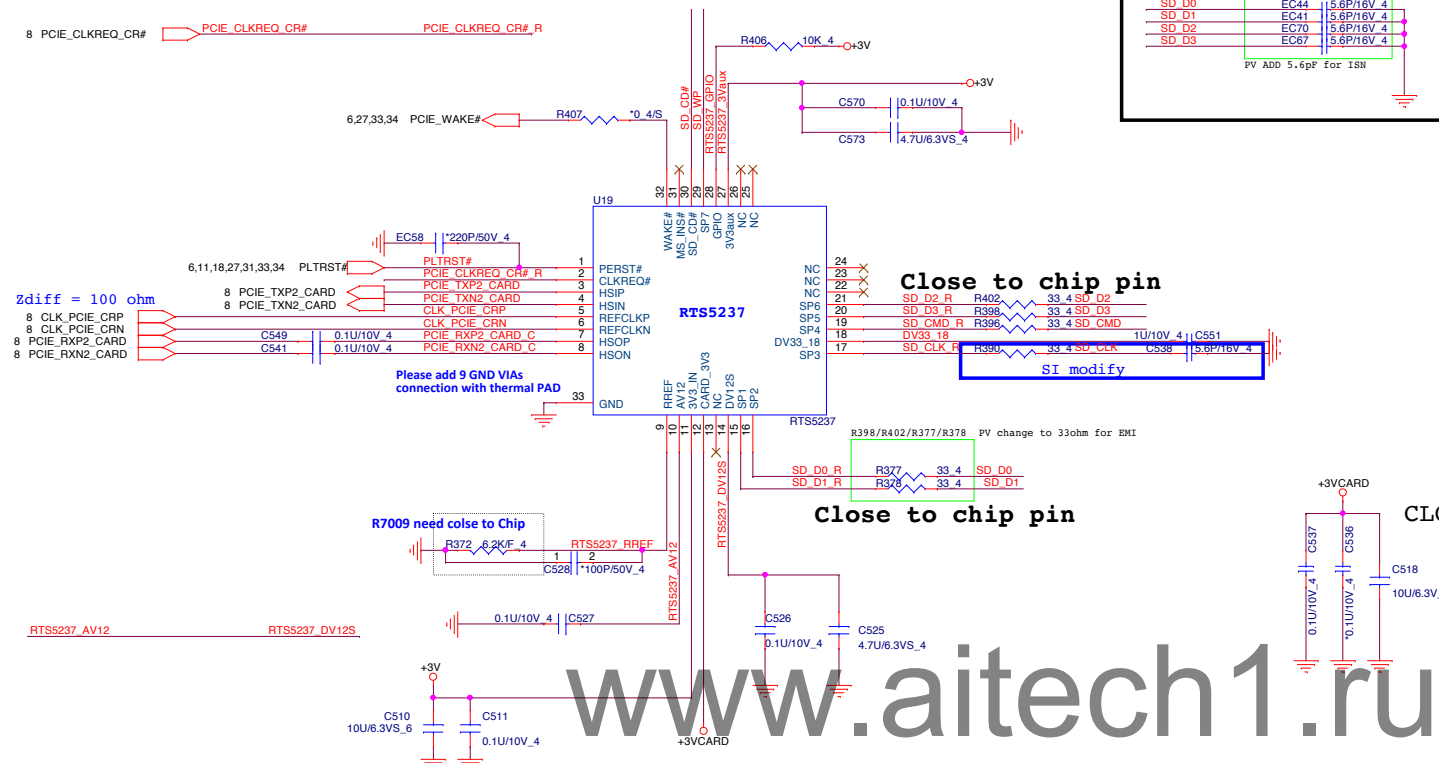


For GIGA  
Stuff Cc,Cd

For 10/100  
NA: Cc,Cd

Remove For Not Using SWR mode



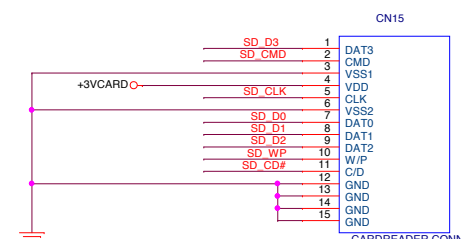


SP1	SD D1	MS D1
SP2	SD D0	MS D0
SP3	SD CLK	MS D0
SP4	SD CMD	MS D2
SP5	SD D3	MS D3
SP6	SD D2	MS CLK
SP7	SD WP	MS BS

Share Pin

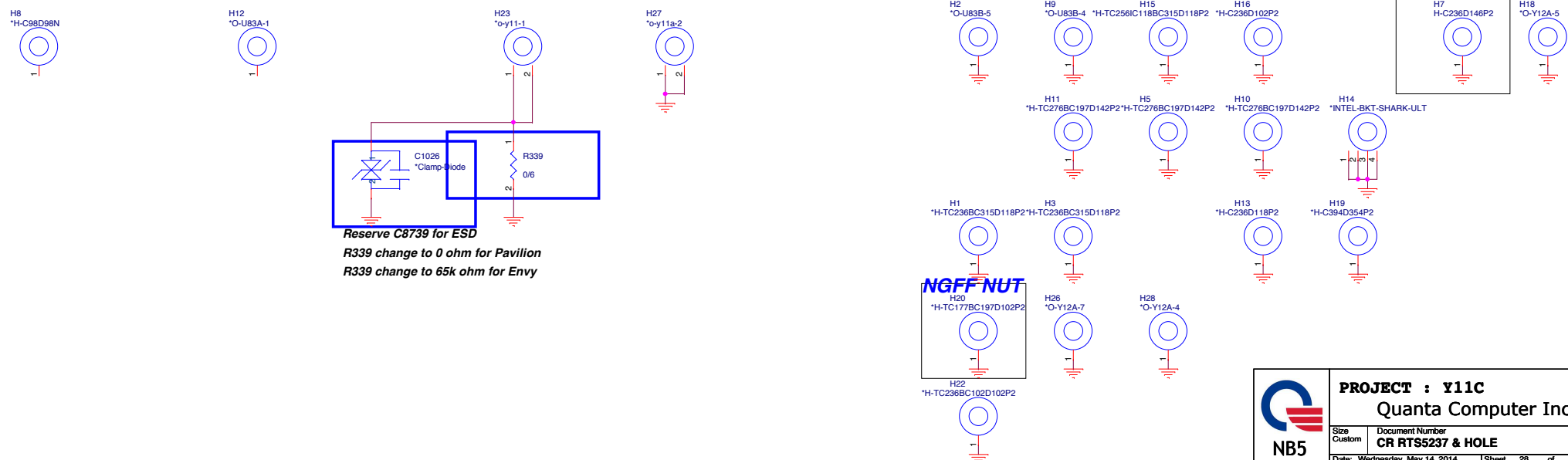
SD / MMC

## CARD READER

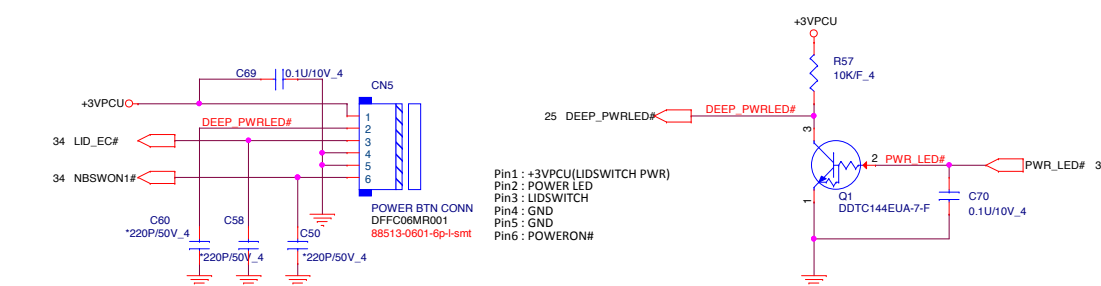


R6x Type

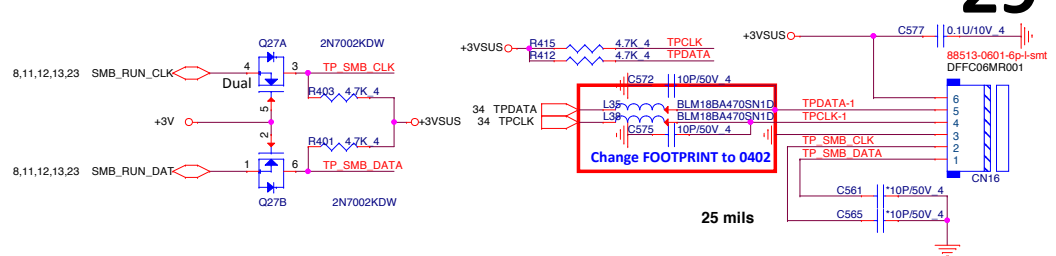
Thermal Nut



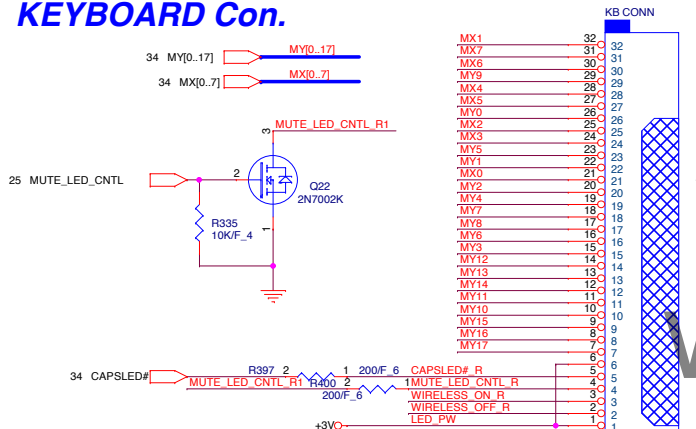
Power Button Connector



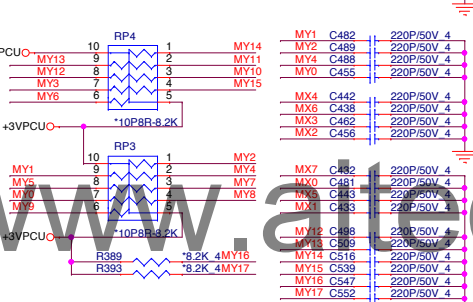
Touch Pad Connector



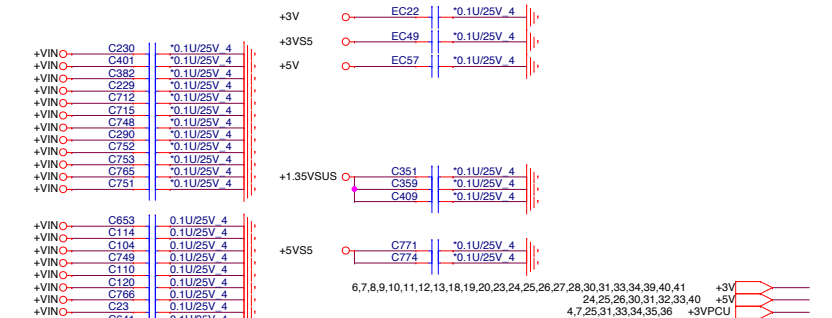
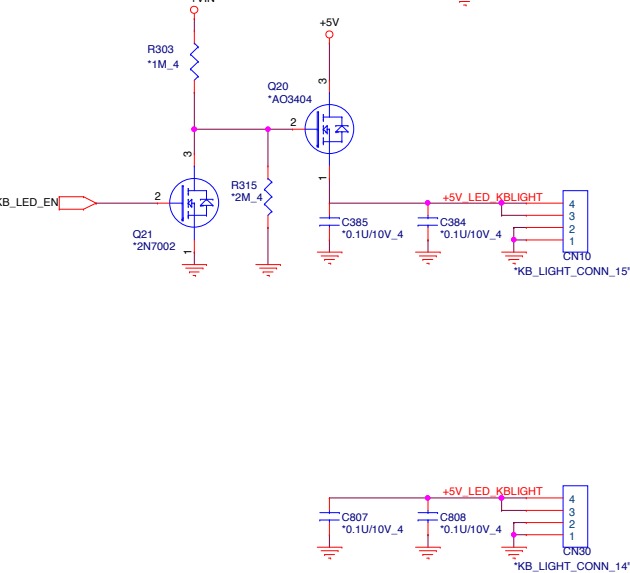
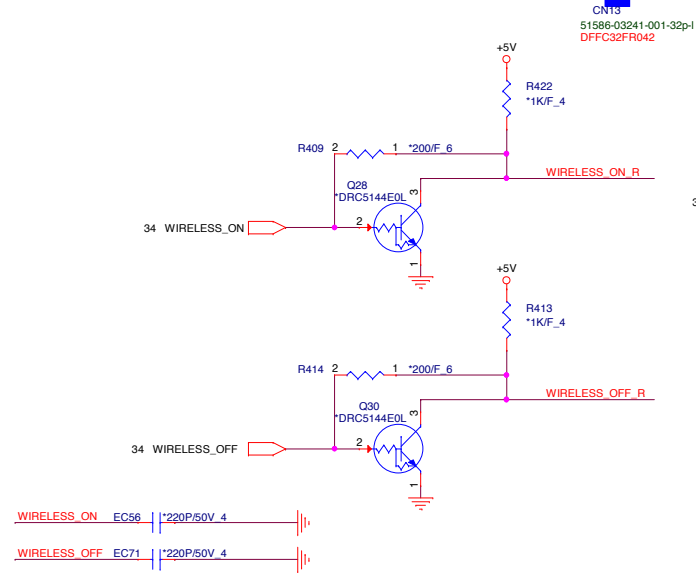
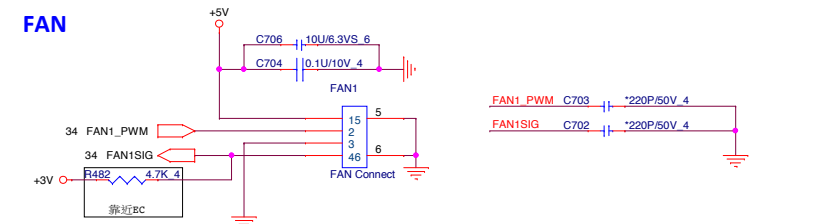
KEYBOARD Con.



KEYBOARD PULL-UP



FAN



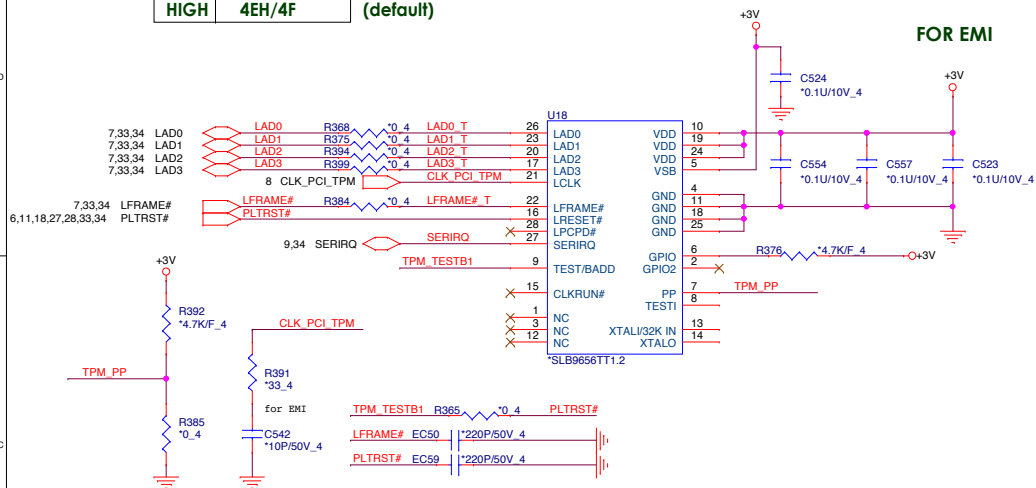




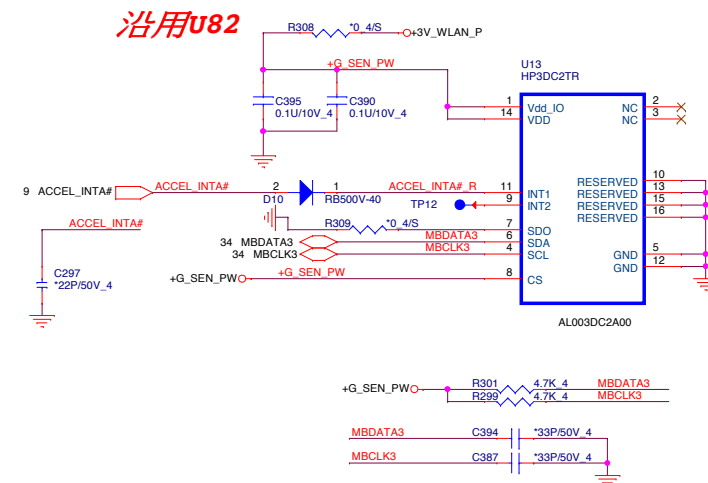
## TPM (1.2)

Address

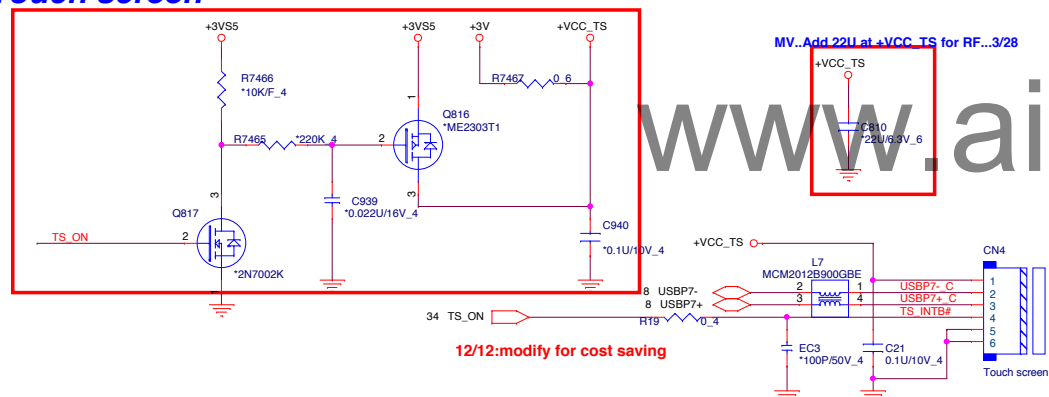
	<b>BADD</b>
<b>HIGH</b>	<b>4EH/4F</b> (default)



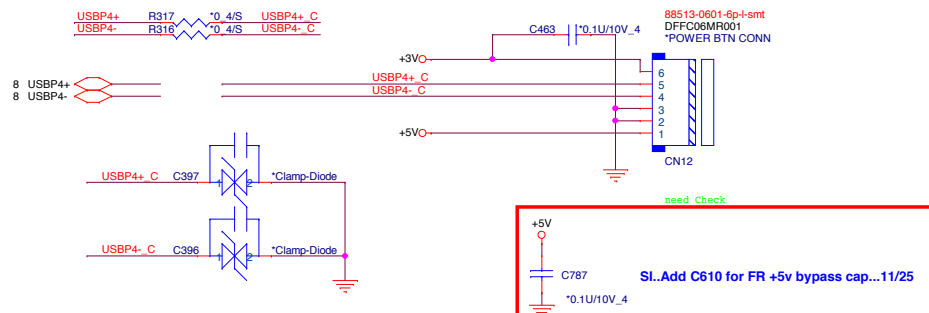
## Accelerometer Sensor



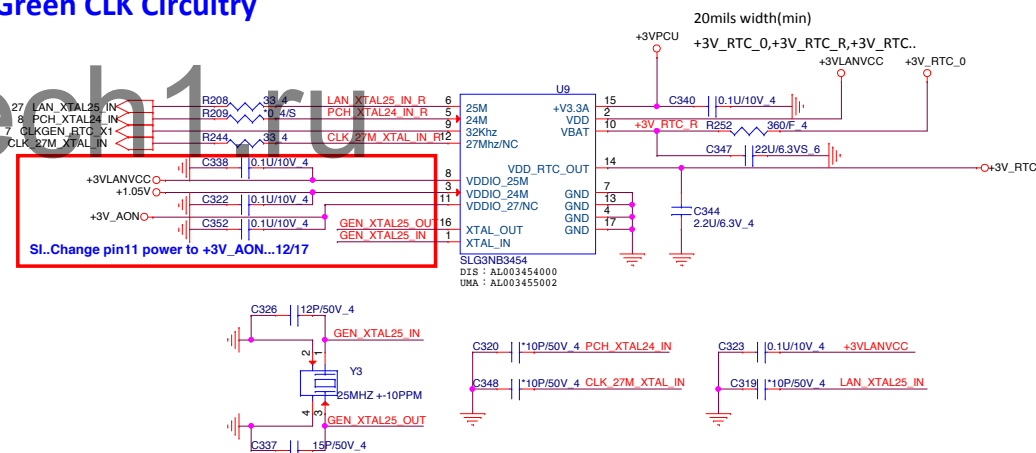
## Touch screen



## Fingerprint Conn

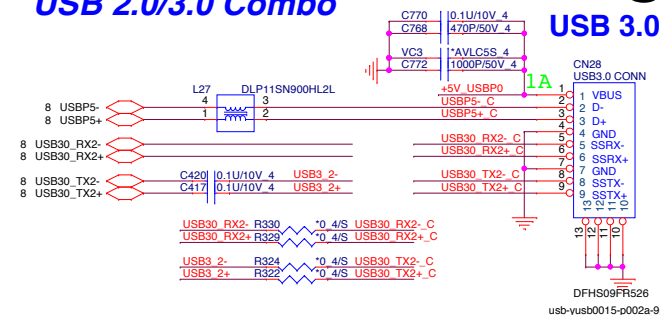
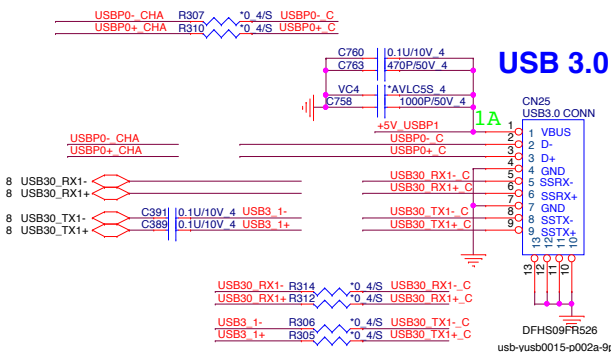


## Green CLK Circuitry

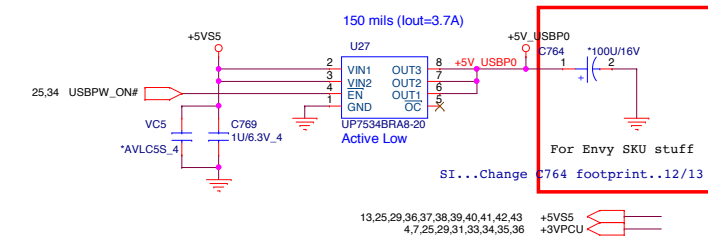
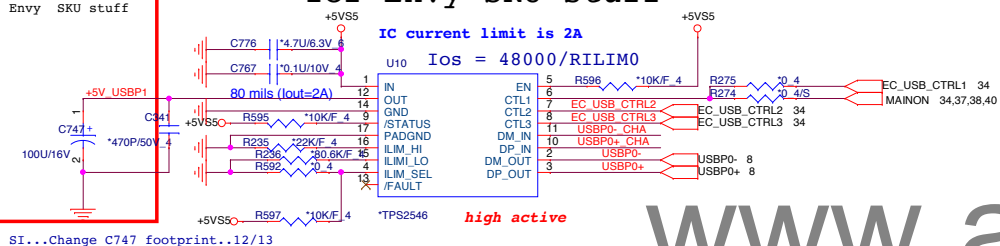


## USB 3.0

## USB 3.0



for Envy SKU stuff



Right-Side USB3.0 Re-Driver

A_EQ1	A_EQ0		A_DE1	A_DE0	
B_EQ1	B_EQ0		B_DE1	B_DE0	
0	0	9.5dB	0	0	3.5dB
0	1	13dB	0	1	no de-emphasis
1	0	4.5dB	1	0	2.7dB
1	1	7.5dB	1	1	5dB

TEST : Low = Normal LFPS swing / Hight =Turn down LFPS swing

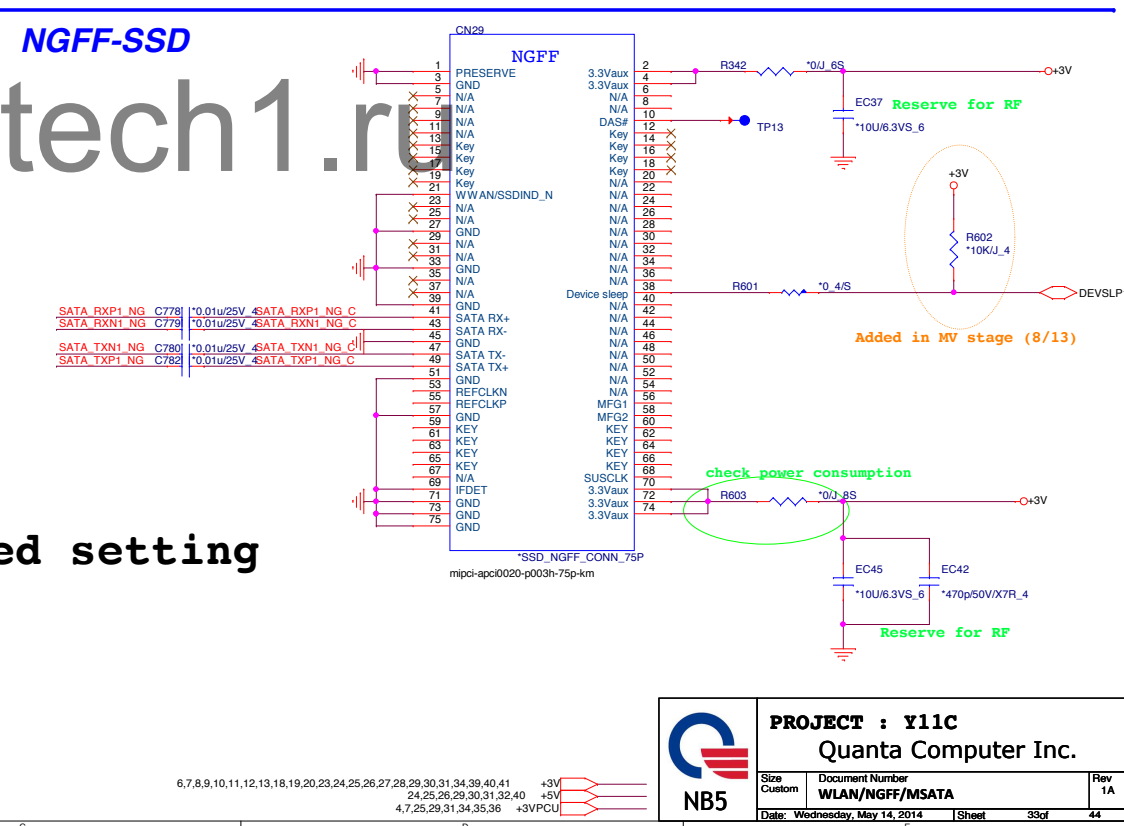
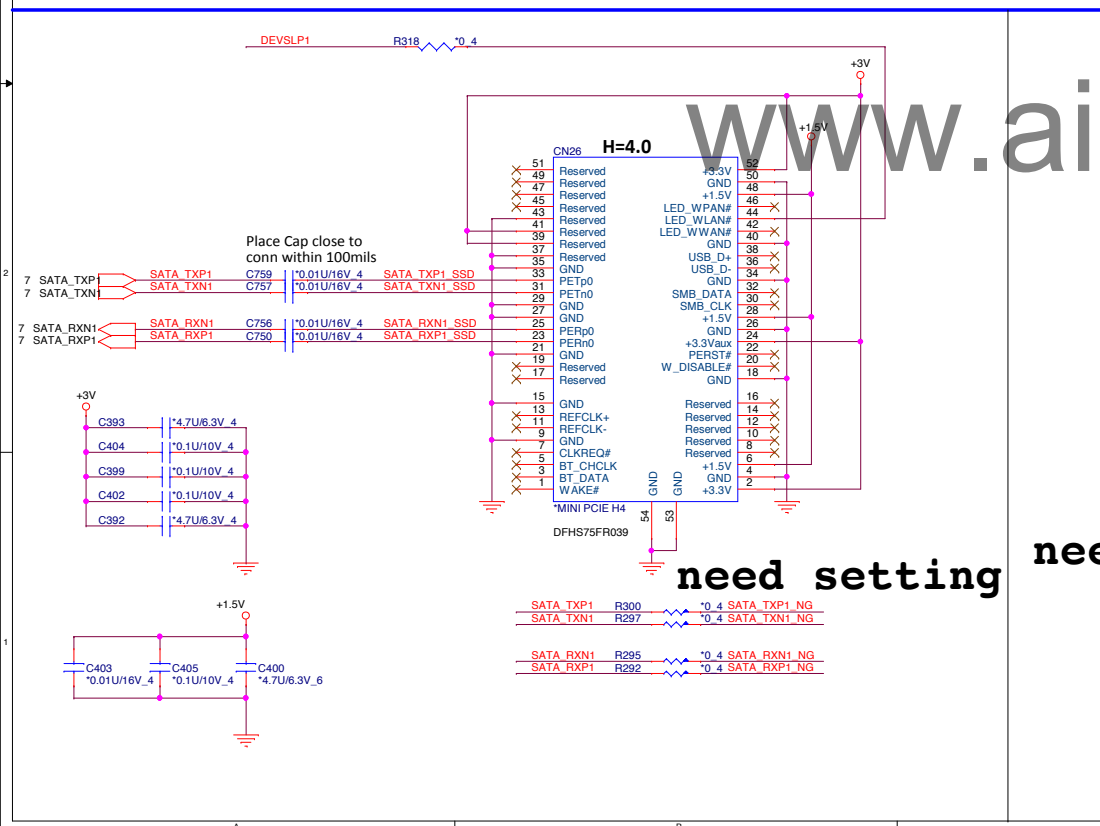
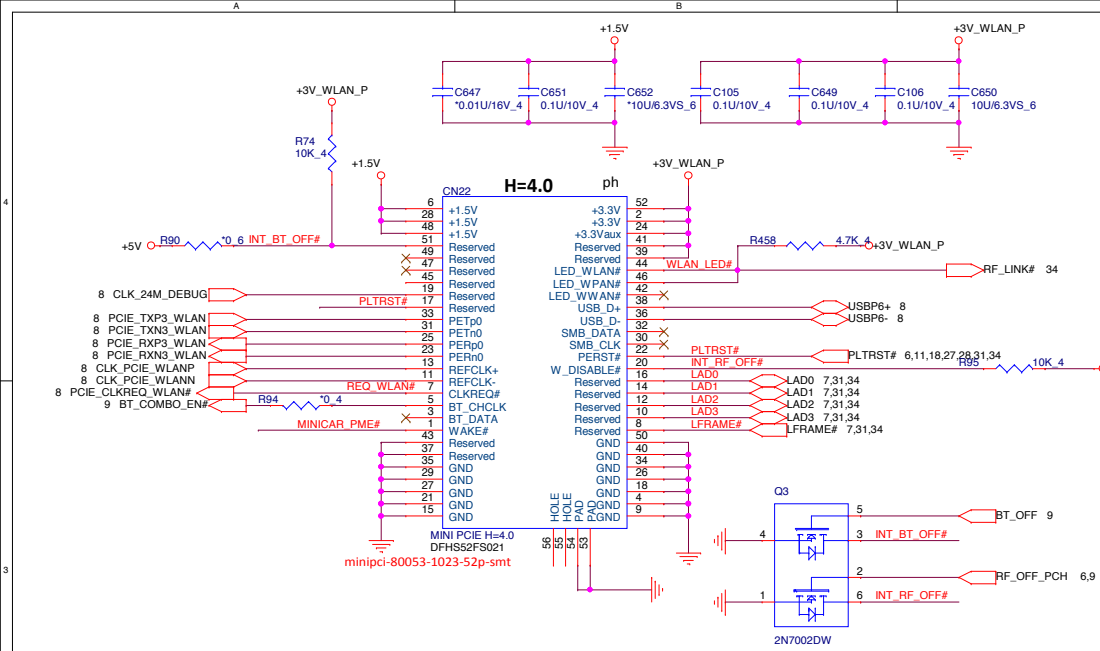
From HOST

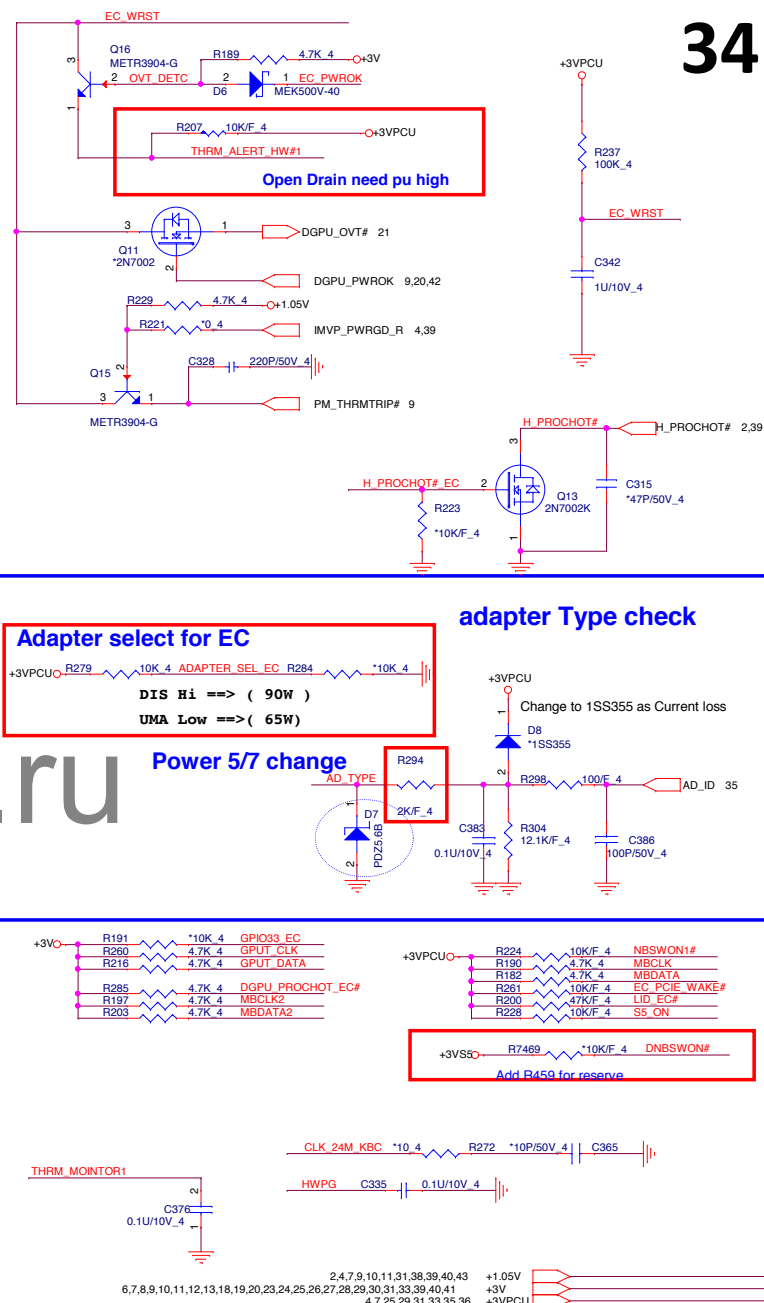
## USB3.0 Re-driver

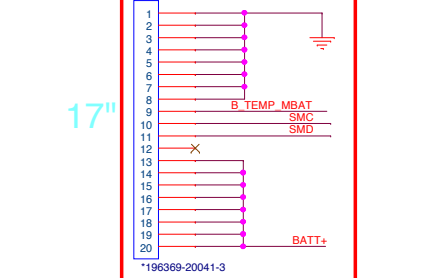
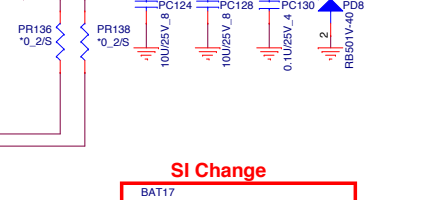
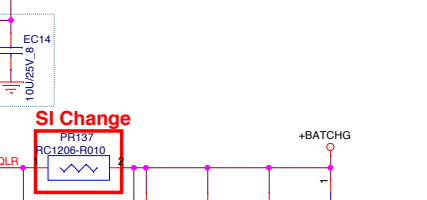
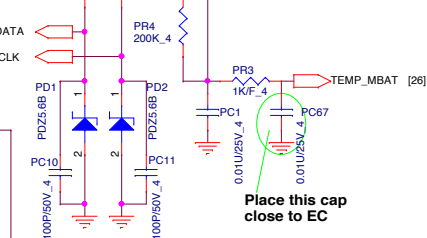
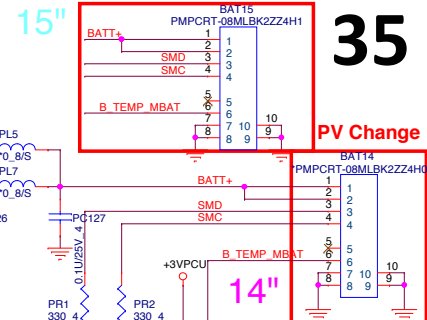
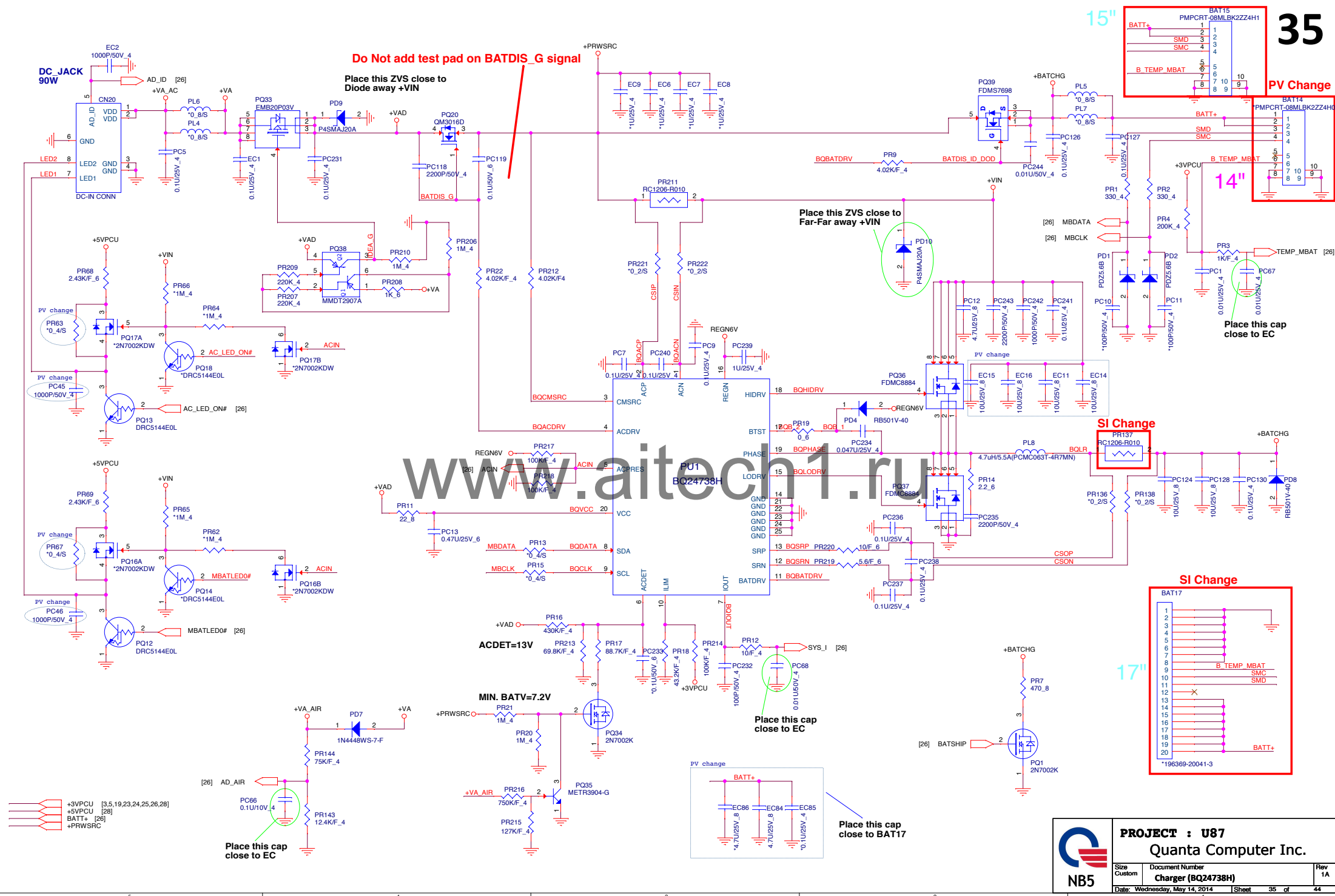
To Connector

DFFC08FR016

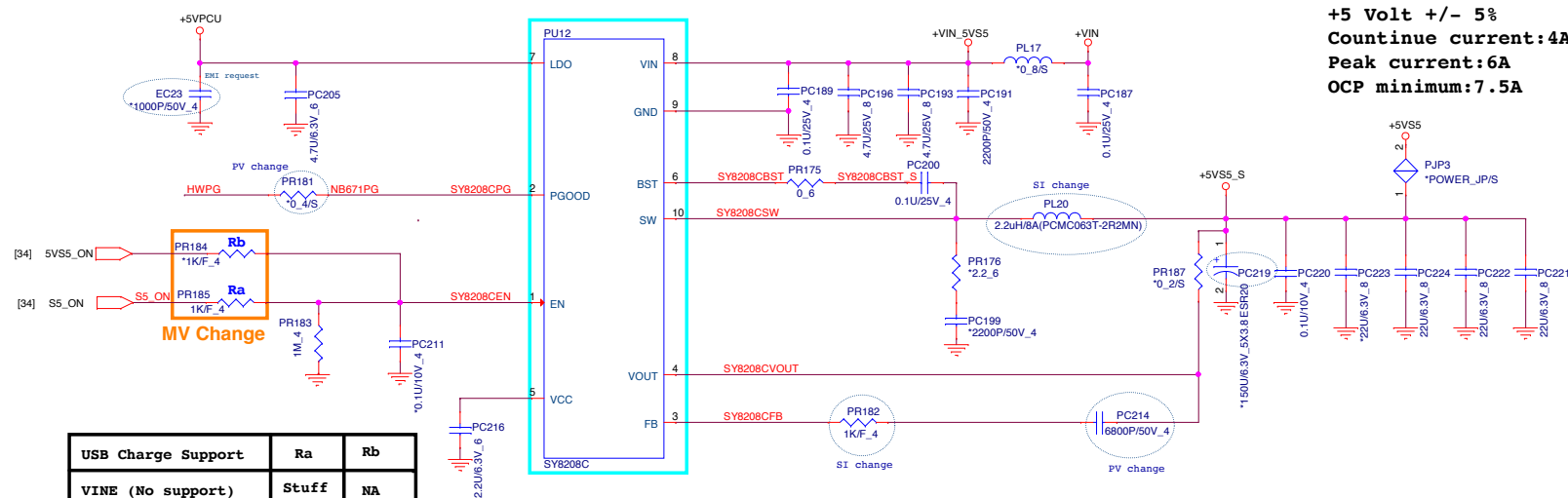
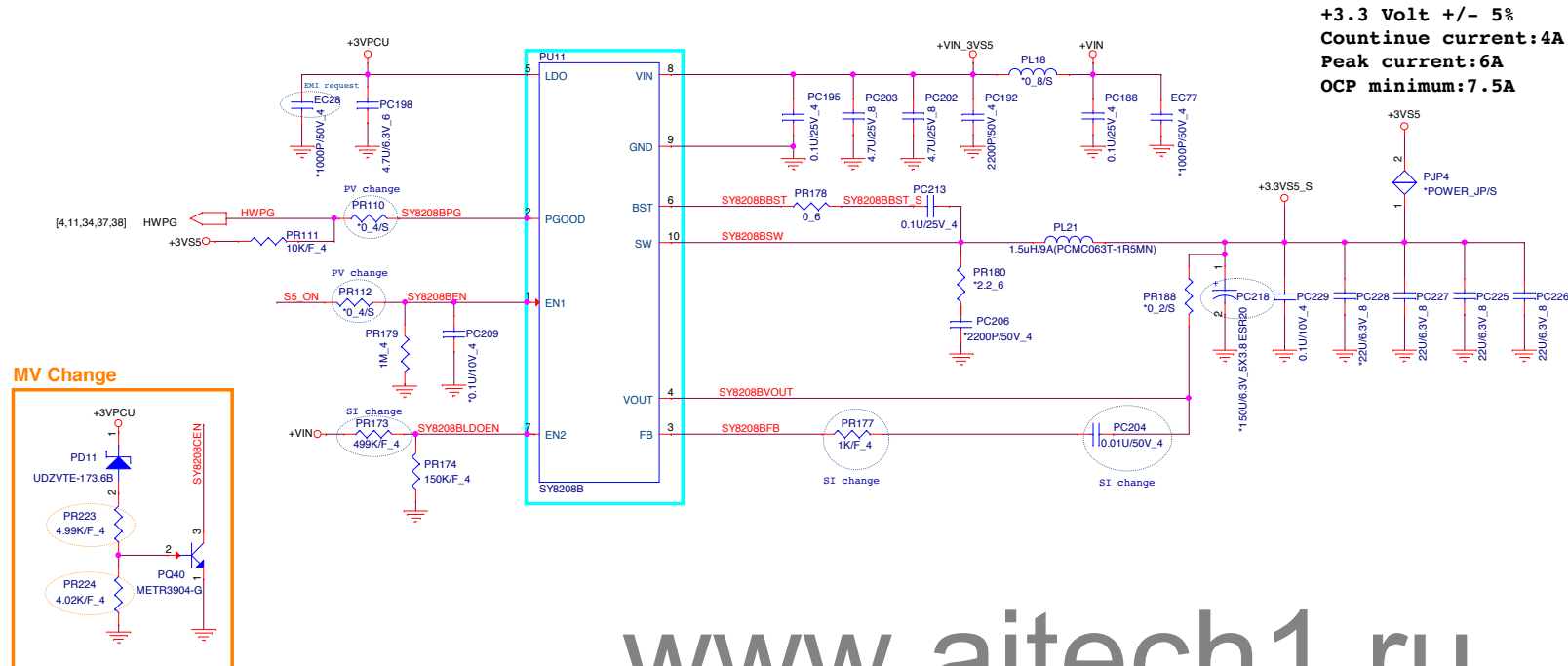
\*Leap Motion







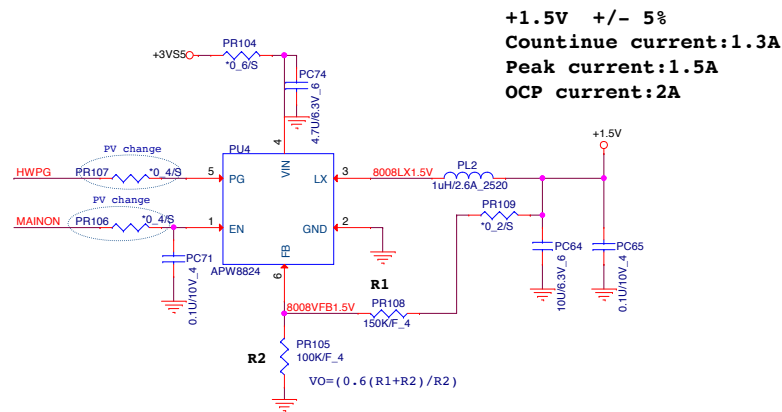
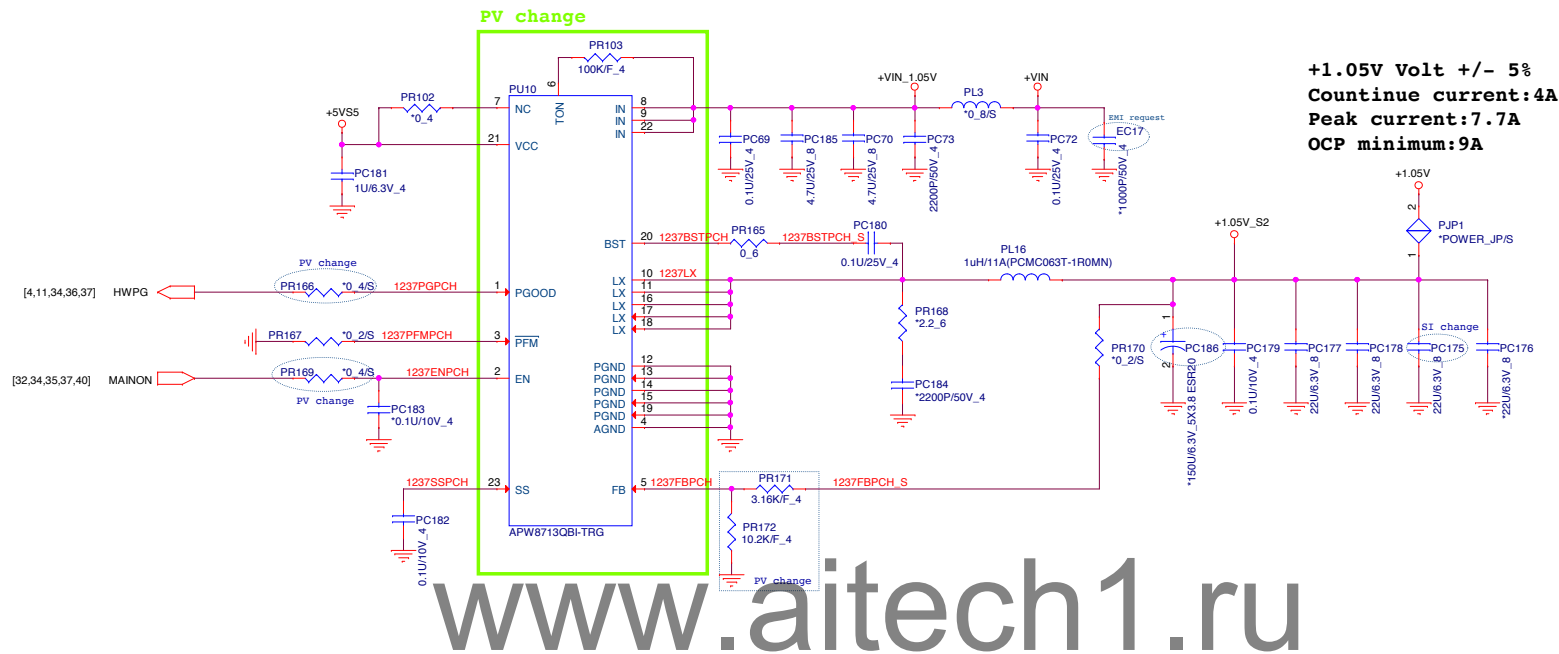
## DC/DC +3VS5/+5VS5



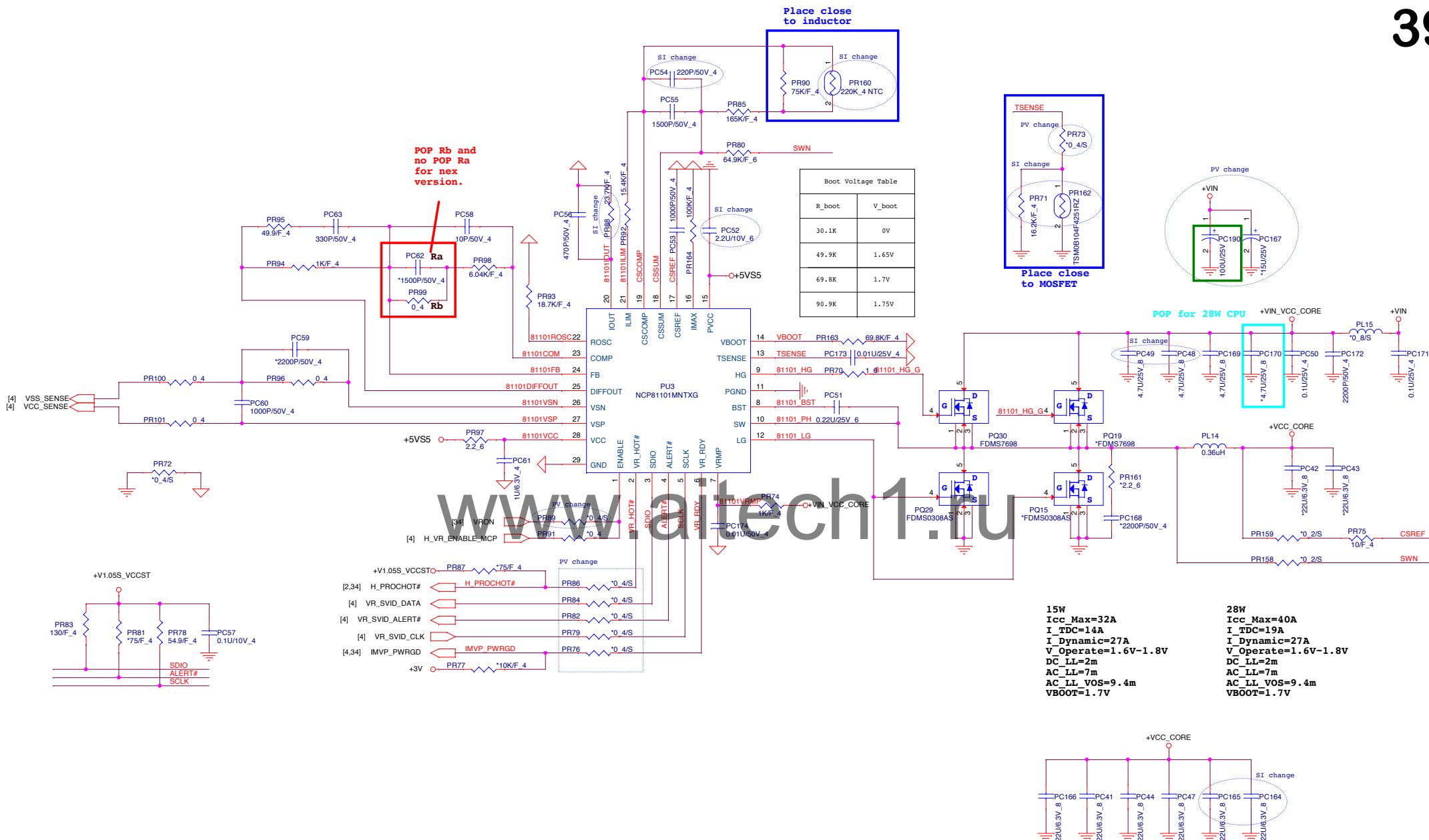
USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support)	NA	Stuff

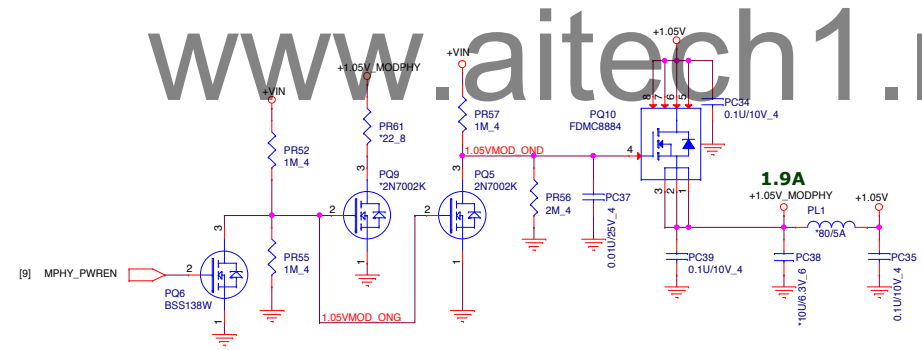
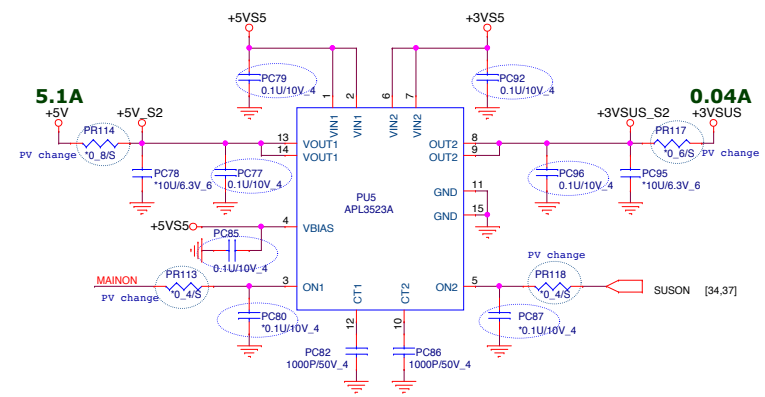
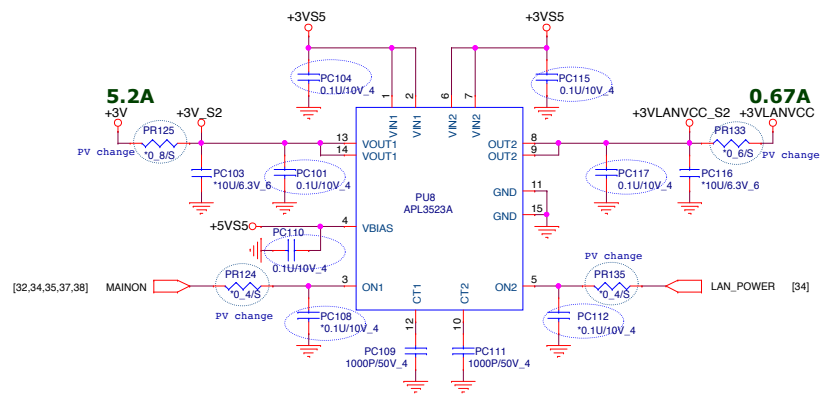






+VIN [24,26,29,30,35,36,37,39,40,41,42,43]  
 +3VS5 [6,7,9,10,11,25,29,32,33,36,40,43]  
 +5VS5 [13,25,29,32,36,37,39,40,41,42,43]



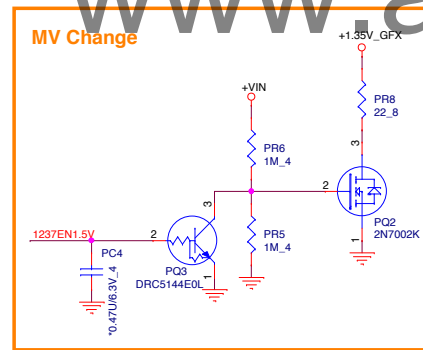
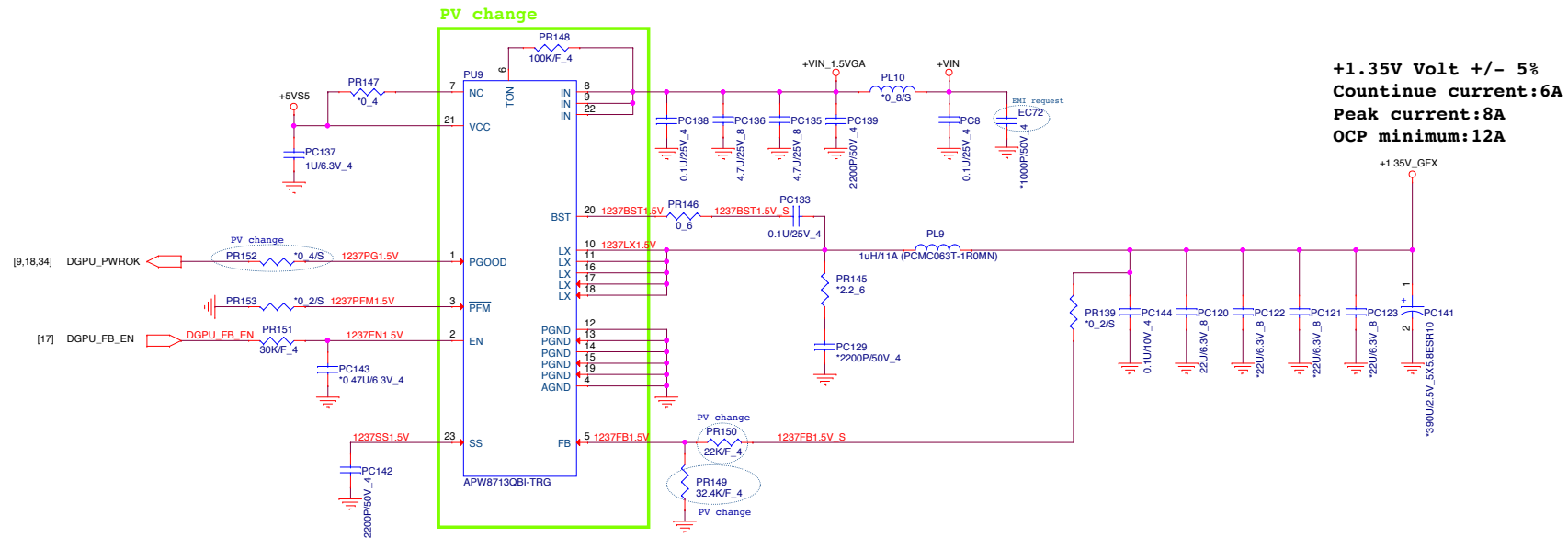


[6,7,8,9,10,11,12,13,14,17,18,23,24,25,26,27,28,29,30,31,33,34,39,41]	+3V
[24,25,26,29,30,31,32,33]	+5V
[24,26,29,30,35,36,37,38,39,41,42,43]	+VIN
[6,7,9,10,11,25,29,32,33,36,38,43]	+3VS5
[13,25,29,32,36,37,38,39,41,42,43]	+3VS5
[27,31]	+3VLANVCC

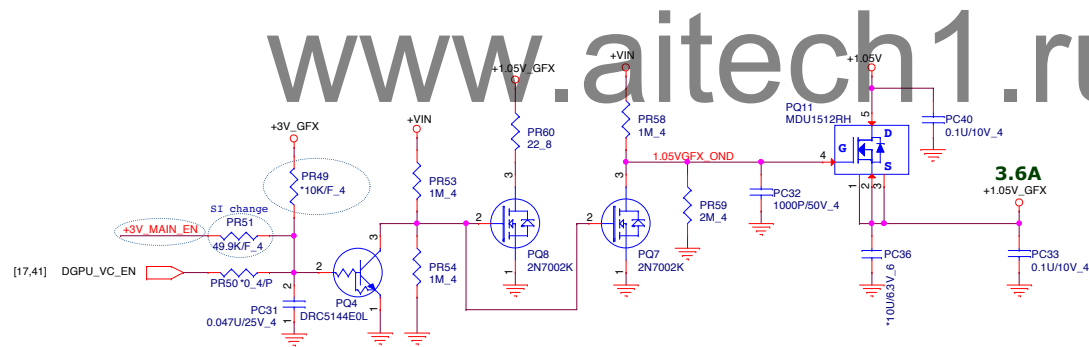
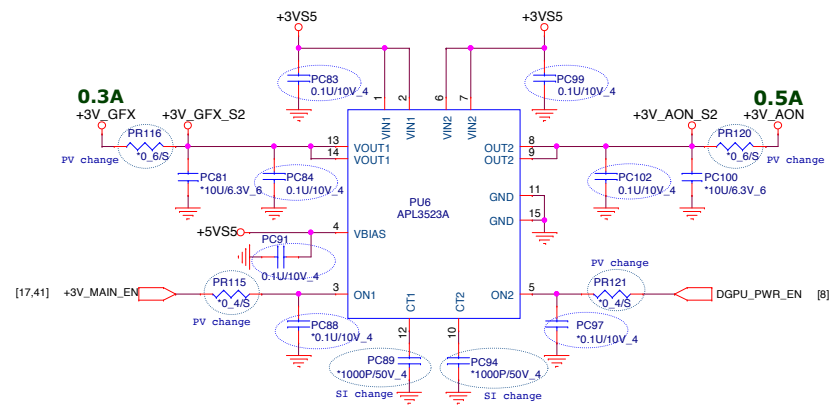
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VGA TYPE	Ca, Cb
N15S-GX (25W)	No stuff
N15P-GT (35W)	Stuff





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Battery Connector	Pavillion	ENVY
14"	DFAD08MR063	DFAD08MR064
15"	DFAD08MR065	DFAD08MR066
17"	DFFC20FR081	DFFC20FR081

USB Charge Support	PR185	PR184
Pavillion	Stuff	NA
ENVY (USB charge)	NA	Stuff

UMA	Disable Page 41 、 42 、 43 ,but keep below location
Page 41	PC161 、 PC162
Page 42	PC138 、 PC144 、 PC4 、 PC148
Page 43	PC84 、 PC102 、 PC88 、 PC97 、 PC40 、 PC33

Discrete	Location	Part Number
N15S (25W)	PR155	CS29532FB10
	PC151 、 PC160	NA
	PQ21 、 PQ23 、 PQ25 、 PQ28	NA
N15P (35W)	PR155	CS31242FB13
	PC151 、 PC160	Stuff
	PQ21 、 PQ23 、 PQ25 、 PQ28	Stuff

Title		
<Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date:	Wednesday, May 14, 2014	Sheet 44 of 44